RTL8318P-LF

16-PORT 10/100M/
1-PORT 10/100/1000M/
1-PORT MII INTERFACE
ETHERNET SWITCH CONTROLLER WITH
EMBEDDED MEMORY

DATASHEET

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2006/02/22	First release.
1.1	2006/04/04	Correct EEPROM description (see Table 35, page 50). Add Absolute Maximum Ratings, page 94. Add pin description of internal pull-up or pull-down (see Table 1, page 7).

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1. General Description

The RTL8318P is a layer-2 switch controller that integrates 1.25Mbits of high-speed SSRAM, an 8K entry MAC address lookup table, 17 Ethernet/Fast Ethernet MACs plus 1 Gigabit MAC, and a switch engine into one chip.

The Remote Management Tool (RMT) software package is bundled with the RTL8318P. The RMT is a Windows-based tool developed to enhance the functionality of Realtek's Pseudo-Managed layer 2 switches via software. The RMT gives network administrators the ability to remotely configure and monitor Pseudo-Managed layer 2 switches as though they were intelligent switches. With QoS, Trunking, VLAN, bandwidth control, remote control, and an 0.18µm process, the RTL8318P is a cost effective switch controller for a 16-Port 10/100+1-port 10/100/1000 Pseudo-managed switch or smart switch or dumb switch application.

Port trunking is supported on all ports to increase bandwidth. Load balancing and fault tolerance provide top performance and reliability. The RTL8318P provides 2-level priority queues for multimedia or real-time network applications. The CoS (Class of Service) can be port-based, IEEE 802.1p tag-based, and/or TCP/IP header TOS/DS field-based. The RTL8318P supports up to 32 VLAN groups that may be configured as port-based VLANs and/or IEEE 802.1Q tagged VLANs. ARP broadcast and Leaky VLAN are also supported.

The RTL8318P supports diagnostics/analysis. Counters are included for: RX byte count, RX packet count, TX byte count, TX packet count, CRC error packet count, collision packet count, dropped packet count, and dropped byte count. The RTL8318P supports TX and RX bandwidth control on each port; 128Kbps, 256Kbps, 512kbps, 1Mbps, 2Mbps, 4Mbps, and 8Mbps may be selected in each direction.

The RTL8318P provides for a Scan LED Group to display each port's status, without extra component cost. A loop-detection function is provided to notify whether a network loop exists, either via a visual LED, or via a register flag for smart applications. LED displays for broadcast storm, trunking status, flow control, and traffic utilization are also provided.

Maximum packet length can be up to 1552 bytes. The RTL8318P supports the ability to drop 802.1D specified reserved group MAC addresses: (01-80-C2-00-00-04 to 01-80-C2-00-00-0F) according to pin strapping upon reset, or register setting. The RTL8318P default setting enables dropping of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause), 01-80-c2-00-00-02 (802.3ad LACP) will always be filtered.

The RTL8318P supports IEEE 802.3x full duplex flow control and back pressure half duplex flow control. Full duplex flow control can be disabled manually or automatically to ensure QoS control or bandwidth control works correctly. Broadcast storm filtering prevents network crashes caused by abnormal broadcast activity.

As well as supporting IEEE 802.3u auto-negotiation, the RTL8318P supports PHY Read/Write registers to access PHY registers through an MDC/MDIO interface. This expands system configuration options. In-band management of the functions provided by the RTL8318P may be implemented using a simple 8051 microprocessor, or via the RTL8318P's RRCP® protocol based Remote Management Tool (RMT).

The RTL8318P is designed with a link-list buffer management architecture and provides 5.4Gbps of bandwidth to achieve wire-speed performance. It also has an intelligent switching engine to prevent Head-of-Line blocking. Only a single 25MHz crystal is required for clock generation.

2. Features

- 16-port 10/100Mbps + 1-port 10/100/1000Mbps + 1-port MII Interface layer-2 Ethernet switch controller with embedded lookup table and packet buffer
- RTL8318P supports 16-port SMII on 10/100Mbps ports and 1-port MII (MAC_Mode) on 10/100Mbps ports.
- RTL8318P supports MII, GMII, on Gigabit-ports
  - Complies with IEEE 802.3ab
  - Half/full duplex for MII
  - Full duplex for GMII
- Built-in 8K entry MAC address lookup table plus 64-entry CAM to eliminate hash collision problems
- Built-in 1.25Mbit SSRAM packet buffer
- Non-blocking wire-speed forwarding and filtering (5.4Gbps throughput)
- Store and forward architecture and head-of-line blocking prevention
- All ports support Speed, Duplex, and 802.3x flow-control ability auto-negotiation
- Supports broadcast storm filtering control
- Supports 802.3x full duplex flow control and back pressure half duplex flow control
- Supports 4-group Trunking function with load balancing and fault tolerance for 10/100M ports
- Supports up to 32 VLAN groups for port-based VLAN and IEEE 802.1Q tag VLAN
- Supports Leaky VLAN
- Two priority queues for three types of Class of Service (CoS)
  - Port-based
  - IEEE 802.1p priority tag
  - TCP/IP header's TOS/DS classifier
- Weighted round robin queue scheduling
- Priority tag insert and remove function
- Supports ASIC based IGMPv1 and IGMPv2 snooping function
- Supports pin strapping, EEPROM, or serial CPU configuration interface
- Supports PHY register read/write access
- Supports Realtek Management Tool (RMT®) for in-band configuration and management
- Supports simple MIB counters
- TX/RX packet/byte, CRC error, and collision counter for diagnostics/statistics
- Supports per-port bandwidth control
- Supports loop detection and indication function
- Provides Scan LED, serial LED and parallel LED interface for port properties and diagnostic display
- Provide Write EEPROM function via software (RMT® or MPU) for Smart Switch application.
- Provide configurable Port Mirror function.
- Needs only one low cost 25MHz crystal or OSC input
- 0.18µm, 128-pin PQFP, 3.3V single power, 5V I/O tolerance

3. System Applications

- 16-Port 10/100/1-Port 10/100/1000/1-Port MII Interface Ethernet Switch Controller for dumb or smart switch application.

In-band management of the functions provided by the RTL8318P may be implemented using a simple 8051 microprocessor, or via the RTL8318P's RRCP® protocol based Remote Management Tool (RMT).

4. Block Diagram

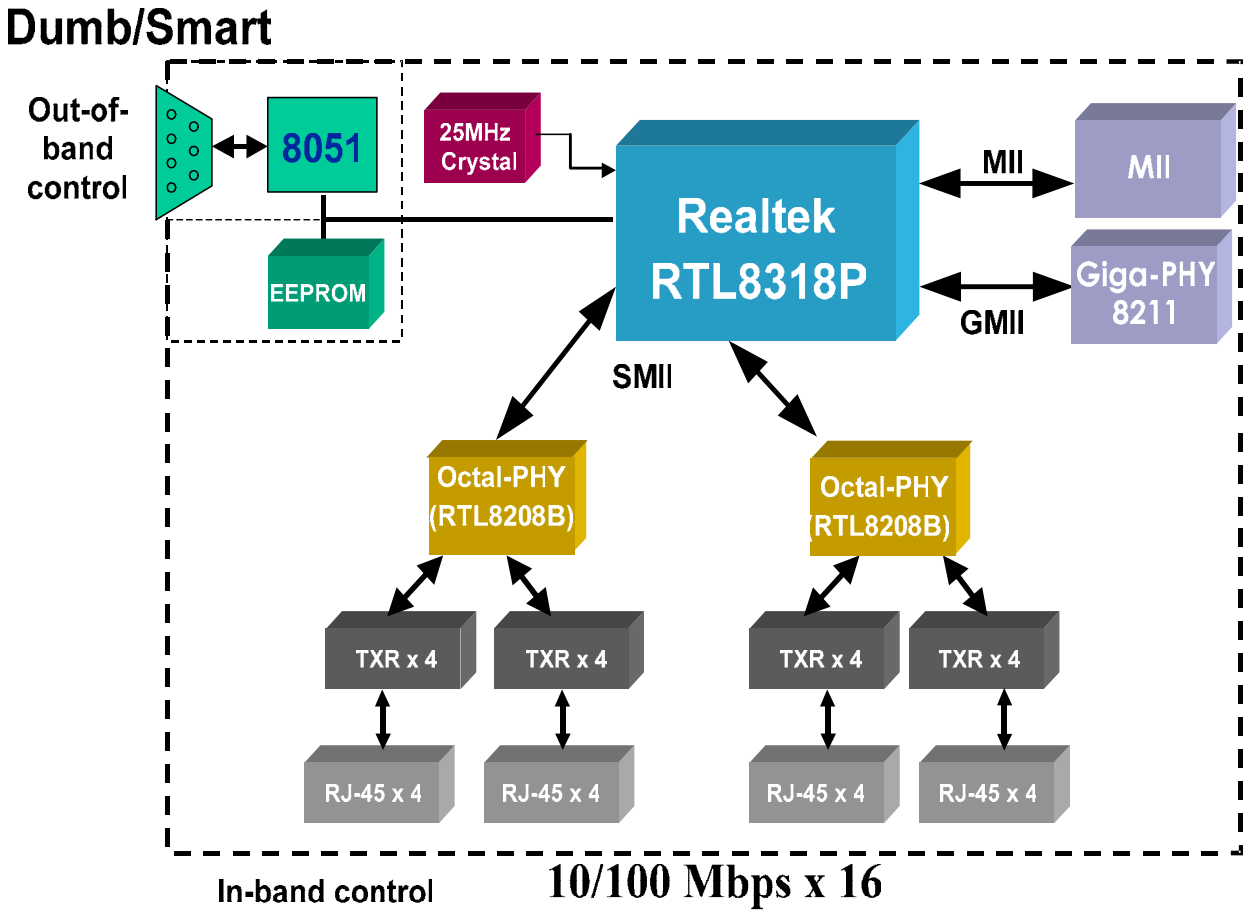


Figure 1. Block Diagram

5. Functional Block Diagram

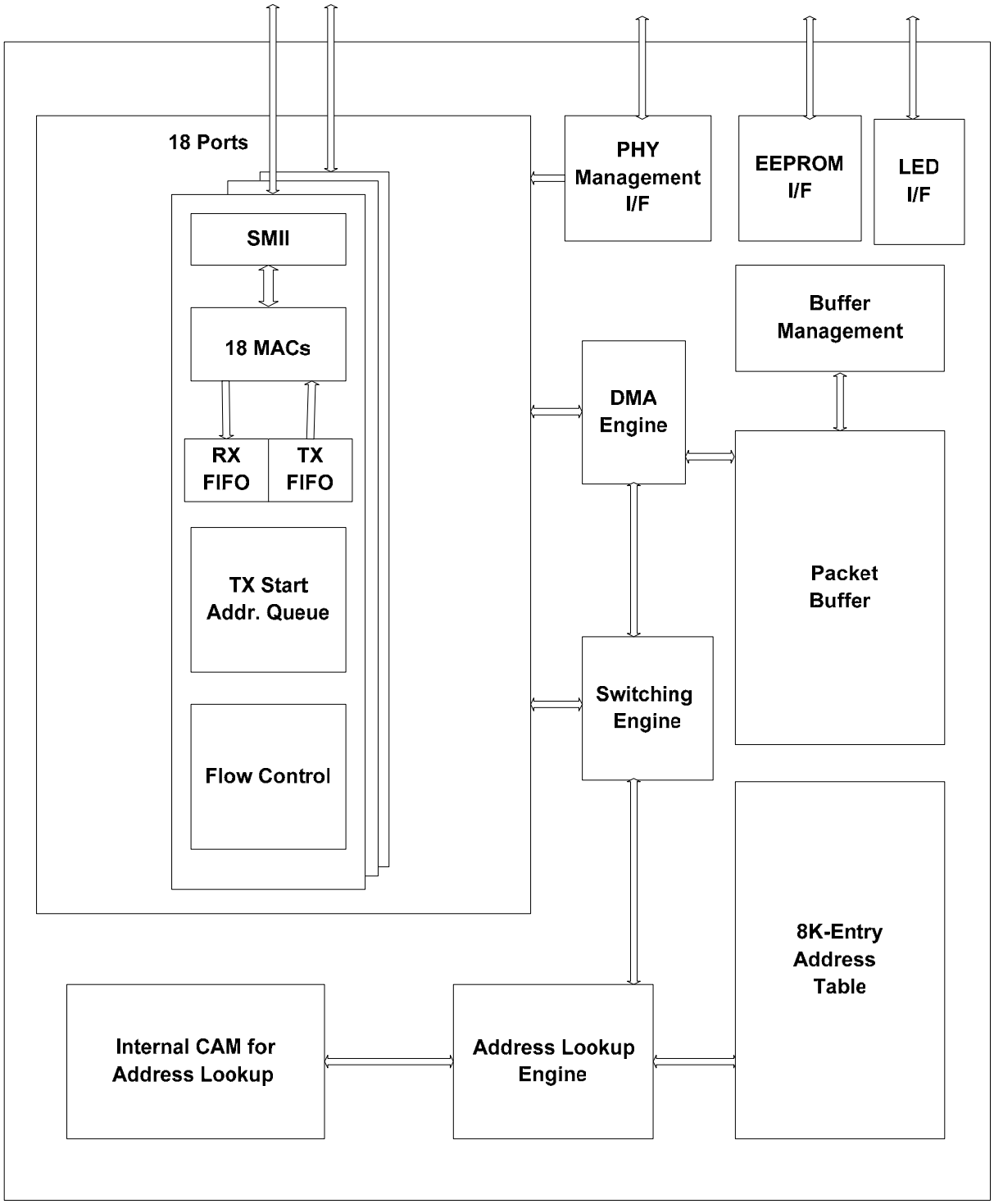


Figure 2. Functional Block Diagram

6. Pin Assignments

6.1. Pin Assignments with MII Interface (set pin12, EnMII = 1)

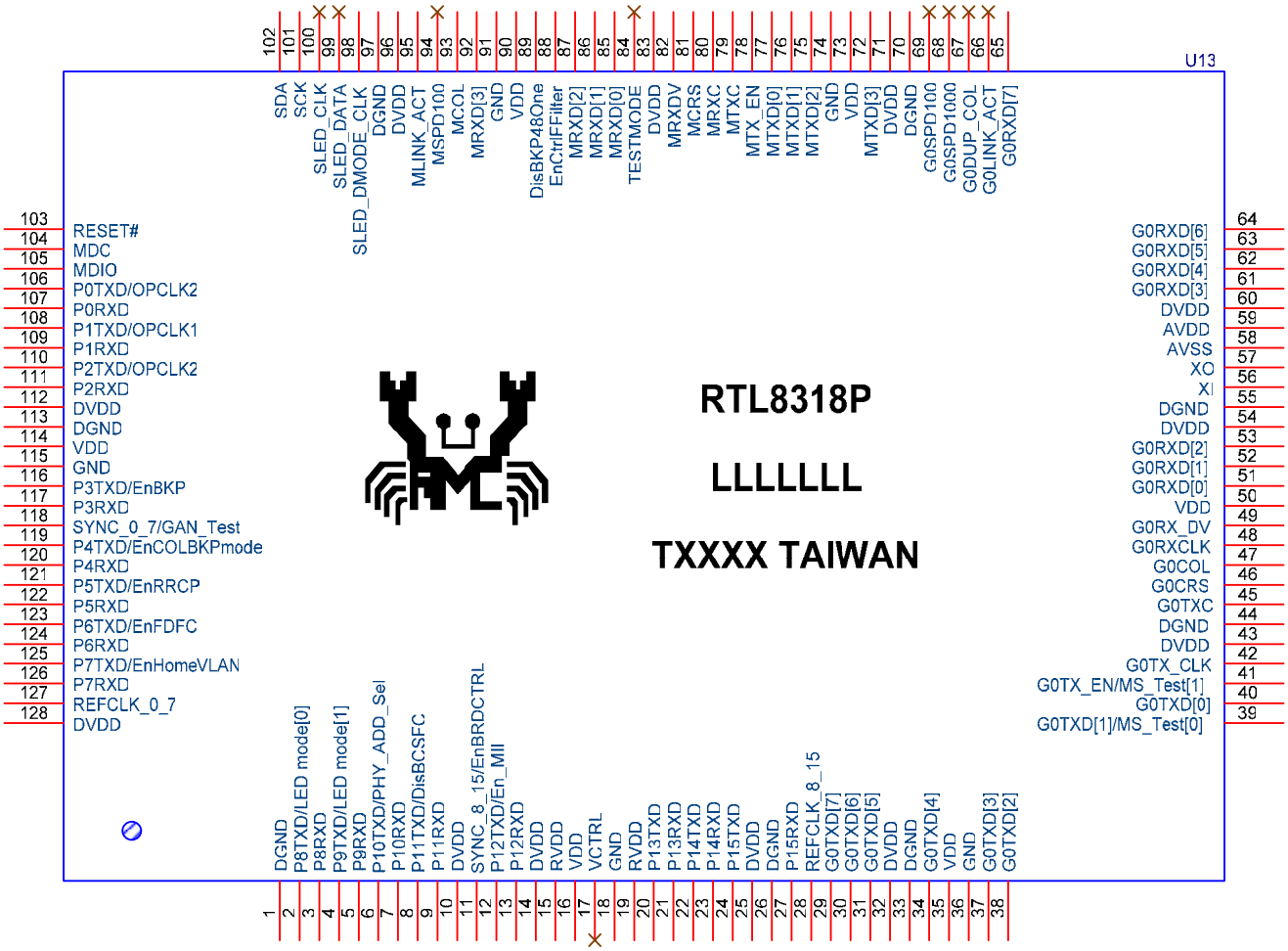


Figure 3. Pin Assignments With MII Interface

6.2. Lead (Pb)-Free Package Identification

Lead (Pb)-free package is indicated by an 'L' in the location marked 'T' in Figure 3.

6.3. Pin Assignments with Scan_LED (set pin12, EnMII = 0)

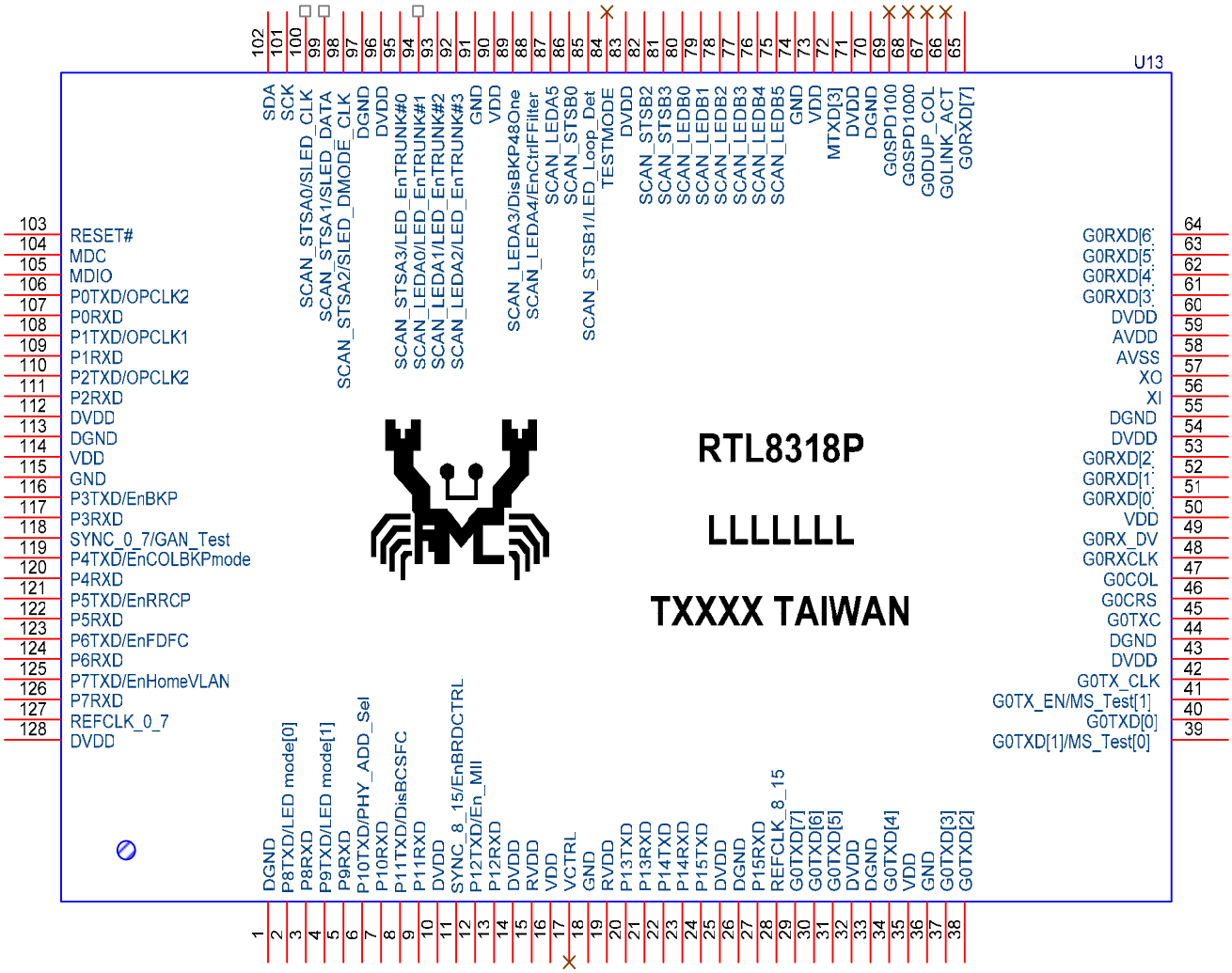


Figure 4. Pin Assignments With Scan_LED

6.4. Lead (Pb)-Free Package Identification

Lead (Pb)-free package is indicated by an 'L' in the location marked 'T' in Figure 4.

6.5. Pin Assignment Table (128-Pin PQFP)

Type codes used: P = Power; G = Ground, I = Input, O = Output. PU = Internal pull-up. PD = Interanl pull-down. Internal resistor = 40KΩ

Table 1. Pin Assignment Table

Pin #	RTL8318P with MII Signal Name	RTL8318P with SCAN_LED Signal Name	HW pin Strapping Function	TYPE	Pin #	RTL8318P with MII Signal Name	RTL8318P with SCAN_LED Signal Name	HW pin Strapping Function	TYPE
1	DGND	DGND		G	43	DVDD	DVDD		P
2	P8TXD	P8TXD	LED mode[0]	I/O_{PU}	44	DGND	DGND		G
3	P8RXD	P8RXD		I_{PD}	45	G0TXC	G0TXC		O_{PD}
4	P9TXD	P9TXD	LED mode[1]	I/O_{PD}	46	G0CRS	G0CRS		I_{PD}
5	P9RXD	P9RXD		I_{PU}	47	G0COL	G0COL		I_{PD}
6	P10TXD	P10TXD		O_{PU}	48	G0RXCLK	G0RXCLK		I_{PD}
7	P10RXD	P10RXD	PHY_ADD_ Sel	I_{PD}	49	G0RX_DV	G0RX_DV		I_{PD}
8	P11TXD	P11TXD	DisBCSFC	O_{PD}	50	VDD	VDD		P
9	P11RXD	P11RXD		I_{PD}	51	G0RXD[0]	G0RXD[0]		I_{PD}
10	DVDD	DVDD		P	52	G0RXD[1]	G0RXD[1]		I_{PD}
11	SYNC_8_15	SYNC_8_15	EnBRDCTRL	I/O_{PD}	53	G0RXD[2]	G0RXD[2]		I_{PD}
12	P12TXD	P12TXD	En_MII	O_{PD}	54	DVDD	DVDD		P
13	P12RXD	P12RXD		I_{PD}	55	DGND	DGND		G
14	DVDD	DVDD		P	56	XI	XI		I
15	RVDD	RVDD		P	57	XO	XO		O
16	VDD	VDD		P	58	AVSS	AVSS		G
17	VCTRL	VCTRL		O	59	AVDD	AVDD		P
18	GND	GND		G	60	DVDD	DVDD		P
19	RVDD	RVDD		P	61	G0RXD[3]	G0RXD[3]		I_{PU}
20	P13TXD	P13TXD		O_{PD}	62	G0RXD[4]	G0RXD[4]		I_{PU}
21	P13RXD	P13RXD		I_{PD}	63	G0RXD[5]	G0RXD[5]		I_{PU}
22	P14TXD	P14TXD		O_{PD}	64	G0RXD[6]	G0RXD[6]		I_{PU}
23	P14RXD	P14RXD		I_{PD}	65	G0RXD[7]	G0RXD[7]		I_{PU}
24	P15TXD	P15TXD		O_{PD}	66	G0LINK_ACT	G0LINK_ACT		O_{PU}
25	DVDD	DVDD		P	67	G0DUP_COL	G0DUP_COL		O_{PU}
26	DGND	DGND		G	68	G0SPD1000	G0SPD1000		O_{PU}
27	P15RXD	P15RXD		I_{PD}	69	G0SPD100	G0SPD100		O_{PU}
28	REFCLK_8_ 15	REFCLK_8_ 15		O_{PD}	70	DGND	DGND		G
29	G0TXD[7]	G0TXD[7]		O_{PD}	71	DVDD	DVDD		P
30	G0TXD[6]	G0TXD[6]		O_{PD}	72	MTXD[3]	NC		O_{PU}
31	G0TXD[5]	G0TXD[5]		O_{PD}	73	VDD	VDD		P
32	DVDD	DVDD		P	74	GND	GND		G
33	DGND	DGND		G	75	MTXD[2]	SCAN_LEDB5		O_{PU}
34	G0TXD[4]	G0TXD[4]		O_{PD}	76	MTXD[1]	SCAN_LEDB4		O_{PD}
35	VDD	VDD		P	77	MTXD[0]	SCAN_LEDB3		O_{PD}
36	GND	GND		G	78	MTXEN	SCAN_LEDB2		O_{PD}
37	G0TXD[3]	G0TXD[3]		O_{PU}	79	MTXC	SCAN_LEDB1	MaxPauseCnt(note)	I/O_{PD}
38	G0TXD[2]	G0TXD[2]		O_{PD}	80	MRXC	SCAN_LEDB0		O_{PU}
39	G0TXD[1]	G0TXD[1]	MS_Test[0]	I/O_{PU}	81	MCRS	SCAN_STSB3		O_{PU}
40	G0TXD[0]	G0TXD[0]		I_{PU}	82	MRXDV	SCAN_STSB2		O_{PU}
41	G0TXEN	G0TXEN	MS_Test[1]	I/O_{PU}	83	DVDD	DVDD		P
42	G0TXCLK	G0TXCLK		O_{PU}	84	TESTMODE	TESTMODE		O

Pin #	RTL8318P with MII Signal Name	RTL8318P with SCAN_LED Signal Name	HW pin Strapping Function	TYPE	Pin #	RTL8318P with MII Signal Name	RTL8318P with SCAN_LED Signal Name	HW pin Strapping Function	TYPE
85	MRXD[0]	SCAN_STSB1/LED_Loop_Det		O_{PU}	**107**	P0RXD	P0RXD		I_{PD}
86	MRXD[1]	SCAN_STSB0		O_{PU}	**108**	P1TXD	P1TXD	OPCLK1	I/O_{PD}
87	MRXD[2]	SCAN_LEDA5	MaxPktLen (note)	I/O_{PD}	**109**	P1RXD	P1RXD		I_{PD}
88	EnCtrlFFilter	SCAN_LEDA4	EnCtrlFFilter	I/O_{PD}	**110**	P2TXD	P2TXD	OPCLK0	I/O_{PD}
89	DisBKP48One	SCAN_LEDA3	DisBKP48One	I/O_{PU}	**111**	P2RXD	P2RXD		P
90	VDD	VDD		P	**112**	DVDD	DVDD		G
91	GND	GND		G	**113**	DGND	DGND		G
92	MRXD[3]	SCAN_LEDA2/LED_EnTRUNK#3		I/O_{PU}	**114**	VDD	VDD		P
93	MCOL	SCAN_LEDA1/LED_EnTRUNK#2		I/O_{PU}	**115**	GND	GND		G
94	MSPD100	SCAN_LEDA0/LED_EnTRUNK#1		O_{PU}	**116**	P3TXD	P3TXD	EnBKP	I/O_{PU}
95	MLINK_ACT	SCAN_STSA3/LED_EnTRUNK#0		O_{PU}	**117**	P3RXD	P3RXD		I_{PU}
96	DVDD	DVDD		P	**118**	SYNC_0_7	SYNC_0_7	GAN_Tst	I/O_{PU}
97	DGND	DGND		G	**119**	P4TXD	P4TXD	EnCOLBKP mode	I/O_{PD}
98	NC	SCAN_STSA2/SLED_DMODE_CLK		O_{PU}	**120**	P4RXD	P4RXD		I_{PD}
99	NC	SCAN_STSA1/SLED_DATA		O_{PU}	**121**	P5TXD	P5TXD	EnRRCP	I/O_{PD}
100	NC	SCAN_STSA0/SLED_CLK		I/O_{PU}	**122**	P5RXD	P5RXD		I_{PD}
101	SCK	SCK		I/O_{PU}	**123**	P6TXD	P6TXD	DisFDFC	I/O_{PU}
102	SDA	SDA		I/O_{PU}	**124**	P6RXD	P6RXD		I_{PD}
103	RESET#	RESET#		O_{PU}	**125**	P7TXD	P7TXD	EnHomeVLAN	I/O_{PD}
104	MDC	MDC		I/O_{PU}	**126**	P7RXD	P7RXD		I_{PD}
105	MDIO	MDIO		O_{PU}	**127**	REFCLK_0_7	REFCLK_0_7		O_{PU}
106	P0TXD	P0TXD	OPCLK2	O_{PD}	**128**	DVDD	DVDD		P

Note: HW Strapping functions 'MaxPktLen' and 'MaxPauseCnt' are useless when the MII interface is enabled. 'MaxPktLen' and 'MaxPauseCnt' may be configured via EEPROM, even when the RTL8318P MII interface is enabled

7. Pin Descriptions

Type codes used: P=Power; G=Ground, I=Input, O=Output, Pu=Internal pull up (40K ohm), Pd=Internal pull down (40K ohm).

7.1. SMII Interface (Port #0 ~ Port #15)

Table 2. SMII Interface (Port #0 ~ Port #15)

Pin Name	Type	Pin No.	Description
P0TXD P1TXD P2TXD P3TXD P4TXD P5TXD P6TXD P7TXD P8TXD P9TXD P10TXD P11TXD P12TXD P13TXD P14TXD P15TXD	O	106 108 110 116 119 121 123 125 2 4 6 8 12 20 22 24	SMII Transmit Data Output: SMII transmit data is formed in 10-bit serial words. Each word contains one data byte (two nibbles of 4B coded data) and two status bits. The SMII operates at 125MHz using a global reference clock (REFCLK) and frame synchronization signal (SYNC). SMII transmit data is input on these pins, where: Ports 0~7 transmit data is sent synchronously to SYNC_0_7 and REFCLK_0_7. Ports 8~15 transmit data is sent synchronously to SYNC_8_15 and REFCLK_8_15.
P0RXD P1RXD P2RXD P3RXD P4RXD P5RXD P6RXD P7RXD P8RXD P9RXD P10RXD P11RXD P12RXD P13RXD P14RXD P15RXD	I	107 109 111 117 120 122 124 126 3 5 7 9 13 21 23 27	SMII Receive Data Input: SMII receive data is input on these pins. Where ports 0~7 receive data is received synchronously to SYNC_0_7 and REFCLK_0_7. Ports 8~15 receive data is received synchronously to SYNC_8_15 and REFCLK_8_15.
SYNC_0_7 SYNC_8_15	O	118 11	SMII Synchronization Output. SMII transmit/receive data 10-bit word frame synchronization. Where: SYNC_0_7 synchronizes data for ports 0~7. SYNC_8_15 synchronizes data for ports 8~15.

Pin Name	Type	Pin No.	Description
REFCLK_0_7 REFCLK_8_15	O	127 28	SMII Reference Clock Output. The SMII reference clock output is a 125MHz +- 50ppm clock used to synchronize the SMII data. Ports 0~7 data is sent or received synchronously to SYNC_0_7. Ports 8~15 data is sent or received synchronously to SYNC_8_15.

7.2. GMII/MII Interface (10/100/1000Mbps Port)

Table 3. GMII/MII Interface (10/100/1000 Mbps Port)

Symbol	Mode	Type	Pin No.	Description
G0TX_CLK Not Used	GMII MII	O	42	Transmit Clock Output (GMII mode). 125MHz transmit clock used for G0TXD[9:0] synchronization.
G0TXD[3:0] G0TXD[3:0]	GMII MII	O	37 38 39 40	Transmit Data Output (GMII mode). Transmits data synchronously to the rising edge of G0TX_CLK. Transmit Data Output (MII mode). Transmits data synchronously to the rising edge of G0TXC.
G0TXD[7:4] Not Used	GMII MII	O	29 30 31 34	Transmit Data Output (GMII mode). Transmits data synchronously to the rising edge of G0TX_CLK.
G0TX_EN G0TX_EN	GMII MII	O	41	Transmit Enable Output (GMII mode). Transmit enable which is sent synchronously to the rising edge of G0TX_CLK. Transmit Enable Output (MII mode). Transmit enable which is sent synchronously to the rising edge of G0TXC.
G0RX_CLK G0RXC	GMII MII	I	48	Receive Clock Input (GMII mode). 125MHz receive clock. Used to synchronize received G0TXD[7:0] data. Receive Clock Input (MII mode). 2.5/25 MHz (10Mbps/100Mbps) receive clock. Used to synchronize received G0RXD[3:0] data.
Leave Unconnected G0TXC	GMII MII	I	45	Transmit Clock Input (MII mode). 2.5/25 MHz (10Mbps/100Mbps) receive clock. The transmit data is sent synchronously on the rising edge of G0TXC.

Symbol	Mode	Type	Pin No.	Description
G0RXD[3:0]	GMII	I	61 53 52 51	Receive Data Input (GMII mode). Receive data that is received synchronously at the rising edge of G0RX_CLK.
G0RXD[3:0]	MII			Receive Data Input (MII mode). Receive data that is received synchronously at the rising edge of G0RXC.
G0RXD[7:4]	GMII	I	65 64 63 62	Receive Data Input (GMII mode). Receive data that is received synchronously at the rising edge of G0RX_CLK.
Not Used	MII			
G0RX_DV	GMII	I	49	Receive Data Valid Input (GMII mode). Receive data valid that is received synchronously at the rising edge of G0RX_CLK.
G0RX_DV	MII			Receive Data Valid Input (MII mode). Receive data valid that is received synchronously at the rising edge of G0RXC.
Not Used	GMII	I	46	Carrier Sense Input (MII mode).
G0CRS	MII			G0CRS is only valid in MII half duplex mode. It is asserted high when a valid carrier is detected on the media.
Not Used	GMII	I	47	Collision Detect Input (MII mode).
G0COL	MII			G0COL is only valid in MII half duplex mode. It is asserted high when a collision is detected on the media.

7.3. MII Interface (10/100Mbps Port)

Table 4. MII Interface (MII Port)

Symbol	Mode	Type	Pin No.	Description
MTXD[3:0]	MII	O	72 75 76 77	Transmit Data Output. Transmits data synchronously to the rising edge of MTXC.
MTX_EN	MII	O	78	Transmit Enable Output. Transmit enable which is sent synchronously to the rising edge of MTXC.
MRXC	MII	I	80	Receive Clock Input. 2.5/25 MHz (10Mbps/100Mbps) receive clock. Used to synchronize received MRXD[3:0] data.
MTXC	MII	I	79	Transmit Clock Input. 2.5/25 MHz (10Mbps/100Mbps) receive clock. The transmit data is sent synchronously on the rising edge of MTXC.
MRXD[3:0]	MII	I	92 87 86 85	Receive Data Input. Receive data that is received synchronously at the rising edge of MRXC.
MRX_DV	MII	I	82	Receive Data Valid Input. Receive data valid that is received synchronously at the rising edge of MRXC.
MCRS	MII	I	81	Carrier Sense Input. MCRS is only valid in MII half duplex mode. It is asserted high when a valid carrier is detected on the media.
MCOL	MII	I	93	Collision Detect Input. MCOL is only valid in MII half duplex mode. It is asserted high when a collision is detected on the media.

7.4. Serial Management Interface (SMI)

Table 5. Serial Management Interface (SMI)

Symbol	Type	Pin No	Description
MDC	O (Pu)	104	Serial Management Data Clock (MDC). MDC typically operates at 730KHz. MDC is in tri-state when RST# is active low.
MDIO	IO (Pu)	105	Serial Management Data Input/Output. MDIO is in tri-state when RST# is active low.

7.5. Serial EEPROM Interface

Table 6. Serial EEPROM Interface

Symbol	Type	Pin No	Description
SCK	IO (Pu)	101	Serial EEPROM interface Clock Output/ Serial CPU Access Clock Input. SCK acts as an output pin after hardware reset for EEPROM read access. When the configuration download from EEPROM is finished, or if the EEPROM does not exist, then the SCLK will act as an input pin driven by an external CPU to access the RTL8318P internal registers. SCLK Frequency: Output: Operates at 100KHz Input: Max limit: 10MHz
SDA	IO (Pu)	102	Serial EEPROM Data Input/Output/Serial CPU Access Data Input/Output. After power on, this pin is EEPROM serial data IO. When the configuration download from EEPROM is finished, or if the EEPROM does not exist, then this pin acts as a serial CPU data IO.

7.6. System Pins

Table 7. System Pins

Symbol	Type	Pin No	Description
RST#	I (Pu)	103	System Reset. Active low to reset the system to a known state. After power-on reset (low to high), the configuration modes from Mode Control Pins (page 14) are strapped and determined.
XI/OSCI	I	56	Crystal Input/Oscillator Input. This is a 25Mhz +-50 ppm crystal input or oscillator input. When crystal is used, a capacitor connected from this pin to ground is recommended.
XO	O	57	Crystal Output. When crystal is used, a capacitor connected from this pin to ground is recommended. When an oscillator is used, keep this pin floating.

7.7. Mode Control Pins

The Mode Control pin values are strapped at power on reset. The strapped values may be updated via EEPROM configuration if it exists. They can also be modified by internal register access from the CPU interface.

Table 8. Mode Control Pins

Strap Pin	Pin No.	Type	Description	H/W Pin	EEPROM
MaxPktLen	SCAN_LEDA5 (87)	I/O (P-down)	Max. Valid Packet Length Control. 0: 1536 bytes (Default) 1: 1552 bytes *Note: This function does not support HW strapping when En_MII =1.*	✔	✔
MaxPauseCnt	SCAN_LEDB1 (79)	I/O (P-down)	Max Pause frame Count for Congestion Control. 0: 128 (Default) 1: Continuous *Note: This function does not support HW strapping when En_MII =1.*	✔	✔
EnCOLBKPmode	P4TXD (119)	I/O (P-down)	Enable Carrier-Based Back Pressure Mode. Half duplex back pressure flow control algorithm selection. 0: Carrier-based back pressure mode (Default) 1: Collision-based back pressure mode	✔	✔
EnRRCP	P5TXD (121)	I/O (P-down)	Enable Realtek Remote Control Protocol Function. 0: Disable RRCP (Default) 1: Enable RRCP	✔	✔
EnCtrlFFilter/	SCAN_LEDA4 (88)	I/O (P-down)	Enable 802.1D Specified Reserved Control Frame Filtering. When network control frames are received with the destination MAC address as the group MAC address: (01-80-C2-00-00-04 ~ 01-80-C2-00-00-0F), the switch will drop the frames if the EnCtrlFilter=1. If EnCtrlFilter=0 the frames will be flooded. 0: Disable Filtering (Default) 1: Enable Filtering	✔	✔

Strap Pin	Pin No.	Type	Description	H/W Pin	EEPROM
EnHomeVLAN	P7TXD (125)	I/O (P-down)	Enable Home-VLAN Configuration. When enabled, the switch will be configured in Home-VLAN mode. The 'Home-VLan topology' is shown below: (1) RTL8318P with MII mode (set HW pin EnMII=1): 0: Disable Home-VLan Function (Default) 1: Enable (set VLAN as 16 VLANs with 1Gigabit+ 1 MII overlapping port). (2) RTL8318P with Scan_LED mode (set HW pin EnMII=0): 0: Disable Home-VLan Function (Default) 1: Enable (set VLAN as 16 VLANs with 1Gigabit overlapping port).	✔	✔
DisFDFC	P6TXD (123)	I/O (P-up)	Global Disable Full Duplex 802.3x Pause Flow Control Ability. Globally disables the 802.3x Pause ability flow control of all ports. 0: Disable 802.3x Pause flow control ability 1: Enable 802.3x Pause flow control ability (Default)	✔	✔
EnBKP/	P3TXD (116)	I/O (P-up)	Global Disable Half Duplex Back Pressure Flow Control Ability. Globally disables the back pressure flow control ability of all ports. 1: Enable back pressure flow control ability (Default) 0: Disable back pressure flow control ability	✔	✔
EnBKP48One/	SCAN_LEDA3 (89)	I/O (P-up)	Enable Back Pressure 48 Pass One Algorithm. When the 48 Pass One algorithm is enabled, the switch will pass one incoming packet for every 48 collisions. 0: Disable 48 Pass One algorithm 1: Enable 48 Pass One algorithm (Default)	✔	✔
DisBCSFC	P11TXD (8)	I/O (P-down)	Disable Broadcast Packet Strict Flood Control. Set to disable broadcast packet (DA: 'FF-FF-FF-FF-FF-FF') strict flood mode and configure to loose flood mode. Strict flood mode will drop all broadcast packets if any one destination port is congested. Loose flood mode allows broadcast packets to be flooded to all non-congested ports. 0: Enable Broadcast Packet Strict Flood (Strict flood mode) (default) 1: Disable Broadcast Packet Strict Flood (Loose flood mode)	✔	✔

Strap Pin	Pin No.	Type	Description	H/W Pin	EEPROM
EnBRDCTRL	SYNC_8_15 (11)	I/O (P-down)	Broadcast Storm Filtering Control. Disables broadcast storm filtering control. 0: Disable Broadcast storm filtering control (Default) 1: Enable Broadcast storm filtering control	✔	✔
LED mode[1:0]	P9TXD P8TXD (4,2)	I/O (P-down, P-up)	RTL8318P LED display mode configuration. 00: Scan LED mode. 01: Serial LED mode (single color) (default) 10: Serial LED mode (bi-color) 11: Reserved.	✔	✔
EN_MII	P12TXD (12)	I/O (Pd)	Enable RTL8318P MII port 0: 16 10/100 port and 1*1G port (default) 1: 16 10/100 port and 1*1G port + MII	✔	✔
PHY_ADD_Sel	P10TXD (6)	I/O (Pu)	To select 10/100Mbps PHY address range. 1: To select 10/100Mbps PHY address range = 16~31, (default) 0: To select 10/100Mbps PHY address range = 8~23, MII port address fixed as 5. 10/100/1000Mbps port PHY address is 2 (default).	✔	✔

7.8. LED Pins

7.8.1. Scan LED Pins

Table 9. Scan LED Pins

Symbol	Pin No.	Type	Description
Port 0_7 Scan_LED Group	SCAN_LEDA5 (87) SCAN_LEDA4 (88) SCAN_LEDA3 (89) SCAN_LEDA2 (92) SCAN_LEDA1 (93) SCAN_LEDA0 (94) SCAN_STSA3 (95) SCAN_STSA2 (98) SCAN_STSA1 (99) SCAN_STSA0 (100)	I/O	Scan LED pins display for port0~port7 link status. In Scan LED mode, this LED group display each port's (1)Speed (2) Link/Active (3) Collision/Duplex status without external TTL.
Port 8_15 Scan_LED Group	SCAN_LEDB5 (75) SCAN_LEDB4 (76) SCAN_LEDB3 (77) SCAN_LEDB2 (78) SCAN_LEDB1 (79) SCAN_LEDB0 (80) SCAN_STSB3 (81) SCAN_STSB2 (82) SCAN_STSB1 (85) SCAN_STSB0 (86)	I/O	Scan LED pins display for port8~port15 link status. In Scan LED mode, this LED group display each port's (1)Speed (2) Link/Active (3) Collision/Duplex status without external TTL.

7.8.2. Serial LED Pins

Table 10. Serial LED Pins

Symbol	Pin No.	Type	Description
SLED_CLK	SCAN_STSA0 (100)	O	Serial LED Shift Clock. In Serial LED mode, when Serial LED mode is enabled, periodically active to enable SLED_DATA shift into external shift register.
SLED_DATA	SCAN_STSA1 (99)	O	Serial LED Data Output. In Serial LED mode, when Serial LED mode is enabled, serial LED data is shifted out when SLED_CLK is active.
SLED_DMODE_CLK	SCAN_STSA2 (98)	I	Serial LED Diagnostic Mode Item Select Control Pulse Input. This is an external signal pulse input signal for diagnostic item selection. The diagnostic LED display item will change whenever there is a signal pulse clock input on this pin. The diagnostic items list and its display sequence is as follows: (1) DisablePort/RxError (active low) On: Port disabled Blinking: Error Packet Received (includes dropped packets) (2) FlowControl/FCActive (active low) On: Flow control ability enabled Blinking: Congestion flow control active (3) TrunkPort/TKFault (active low) On: Trunk Port Blinking: Trunk link fault port (4) HighPriorityPort (active low) On: High priority port (5) LoopDetectPort (active low) On: Loop event detected. (6) BroadcastStormAlarmPort (active low) On: Broadcast Storm detected (7) Reserved. (8) Reserved.

7.8.3. Parallel LED Pins

The parallel LEDs show Gigabit port and MII port link status, Trunk status, and network loop connection fault detection.

Table 11. Parallel LED Pins

Symbol	Pin No.	Type	Description
G0LINK_ACT G0COL_DUP G0SPD1000 G0SPD100	66 67 68 69	O	LED display for Gigabit port status(Active Low)
MLINK_ACT MCOL_DUP MSPD1000 MSPD100	88 89 94 95	O	LED display for MII port status(Active Low)
LED_EnTRUNK#0 LED_EnTRUNK#1 LED_EnTRUNK#2 LED_EnTRUNK#3	95 94 93 92	O	Trunk Port Enabled LED output. 0 (On): Trunk Enabled 1 (Off): Trunk Disabled. The LED blinks to indicate that there is a trunk member port link down. For Serial LED Mode: act as Trunk 0 (port 0~3) Enable LED. For Serial LED Mode: act as Trunk 1 (port 4~7) Enable LED. For Serial LED Mode: act as Trunk 2 (port 8~11) Enable LED. For Serial LED Mode: act as Trunk 3 (port 12~15) Enable LED.
LED_Loop_Det (SCAN_STSB1)	85	O	For Serial LED mode: act as Loop detect for global port. Loop Detect LED output. 0: Loop detected 1: Loop not detected

7.9. Power/Ground Pins

Table 12. Power/Ground Pins

Symbol	Type	Pin No	Description
DVDD	3.3V(I)	10, 14 25, 32 43, 54 60, 71 83, 96, 112, 128	3.3V for I/O digital power.
DGND	GND	1, 26 33, 44 55, 70 97, 113	GND for I/O.
RVDD	3.3V(I)	15, 19	3.3V for internal 3.3V to 1.8V regular power input.
VDD	1.8V(I)	16, 35 50, 73 90, 114	1.8V input for internal test used. Do not supply 1.8V if RVDD is used.
GND	GND	18, 36 74, 91 115	GND for Core power.
VCTRL	1.8V(o)	17	Voltage control: This pin controls a PNP transistor to generate the 1.8V power supply for VDD pins. Normally keep this pin floating.
AVDD	3.3V(I)	59	3.3V for PLL power.
AVSS	GND	58	GND for PLL.

7.10. Test Pins

Table 13. Test Pins

Strap Pin	Pin No.	Type	Description	H/W Pin	EEPROM
EnTestMode	Pin 84	I/O (Pd)	Test pin. Normally not pulled up or down.	✔	NO
MS_Test[1:0]	Pin 41 Pin 39	I/O (P-up)	MS_Test[1]: Must use a 4.7K resistance to pull up to 3.3V. MS_Test[0]: Must use a 4.7K resistance to pull down to GND.	✔	NO
GAN_Test	SYNC_0_7 (118)	I/O	Test pin. Must use a 4.7K resistance to pull up to 3.3V.	✔	NO
OPCLK2	P2TXD (106)	I/O (P-down)	Test pin. Normally not pulled up or down.		
OPCLK1	P1TXD (108)	I/O (P-down)	Test pin. Normally not pulled up or down.		
OPCLK0	P0TXD (110)	I/O (P-down)	Test pin. Normally not pulled up or down.		

8. Functional Description

8.1. Reset

8.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse (44ms) will be generated and the RTL8318P will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the RST# signal
- Auto-load the configuration from EEPROM if EEPROM is detected (approx. 10ms)
- Complete the embedded SSRAM BIST process (approx. 24 ms)
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the serial CPU interface
- Start MDC/MDIO configuration and polling

Note 1: To guarantee register access is valid and correct, the RTL8318P registers should not be accessed before the reset initialization process is finished.

Note 2: The connected PHY should have completed the reset process before the RTL8318P starts the MDC/MDIO configuration and polling process.

8.1.2. Software Reset

The software reset command resets the system control circuit and restarts auto-negotiation. It keeps the user configured settings. Hardware pin strapping, EEPROM auto load, and SSRAM BIST are NOT done when using the software reset command.

8.2. MAC to PHY Interface

The MAC to PHY interface supports SMII for 16 ports and MII for 1 port and GMII for 1 Gigabit port.

8.3. Fast Ethernet Port (SMII Interface)

Ports 0~15 are 10/100M Fast Ethernet ports supporting a Serial Media Independent Interface (SMII). The RTL8318P provides three SMII synchronous 125MHz clock outputs for three octal PHYs.

8.4. Gigabit Ethernet Ports (GMII/MII)

The Gigabit Ethernet ports may be configured as GMII (Gigabit Media Independent Interface), or MII (Media Independent Interface) mode to support 1000Base-T, and 10Base-T/100Base-TX modes.

When configured as a GMII only full-duplex operation is supported. When configured as an MII interface, both full and half-duplex operations are supported.

8.5. Fast Ethernet Port (MII Interface)

The RTL8318P provides one MII (Media Independent Interface) port, which utilizes dual-function pins (combined with SCAN_LED group[A:B] pins, see Figure 3, page 5, and Figure 4, page 6). This function is controlled by hardware strapping: En_MII (12). Default setting is disable MII port (Scan_LED enabled).

8.6. MAC Address Table Search and Learning

The RTL8318P MAC address lookup table consists of an 8K-entry hash table and 64-entry Content Addressable Memory (CAM). The RTL8318P uses the last 13 bits of the MAC address to index the 8K-entry lookup table for address searching and learning. If the mapped location in the 8K entries is occupied, the RTL8318P will compare the destination MAC address with the contents of the CAM for address searching, and store the source MAC address in the CAM for address learning. The 64-entry CAM helps avoid address hash collisions and improves switch performance.

8.7. MAC Table Aging Function

In a dynamic network topology, address aging allows the contents of the address table to always be the most recent and correct. A learned source address entry will be cleared (aged out) if it is not updated by the address learning process within a set aging time period. The default aging timer of the MAC address lookup table is between 200 ~ 300 seconds.

8.8. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length < 64 bytes) and oversize packets (length > maximum length) will be discarded. The maximum packet length may be 1536 or 1552 bytes.

This function is controlled by register 0x0001 [1:0].

Hardware Strapping Pin: MaxPKLen (87).

8.9. IEEE 802.1D Reserved Group Addresses Filtering Control

The RTL8318P supports the ability to drop 802.1D specified reserved group MAC addresses: 01-80-C2-00-00-04 to 01-80-C2-00-00-0F. The default setting disables dropping of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause), 01-80-c2-00-00-02 (802.3ad LACP) will always be filtered. MAC address 01-80-C2-00-00-03 is not filtered.

This function is controlled by register 0x0300 [2].

Hardware Strapping Pin: EnCtrlFFilter (88).

8.10. Backoff Algorithm

The RTL8318P implements the truncated exponential backoff algorithm compliant with the IEEE 802.3 standard. The collision counter is restarted after 16 consecutive collisions.

8.11. Inter-Packet Gap

The Inter-Packet Gap is 9.6µs for 10Mbps Ethernet, 960ns for 100Mbps Fast Ethernet.

The RTL8318P supports Transmit Inter-Packet Gap compensation for the frequency shift tolerance of the on-board oscillator.

This function is controlled by register 0x0001 [2].

8.12. Buffer Management

An embedded 1.25Mbit SSRAM is built-in as a packet storage buffer. To efficiently utilize the packet buffer, the RTL8318P divides the SSRAM into 1280 x 128-byte page-based buffers that are linked by a descriptor link list. For an Ethernet packet, a minimum of one, and maximum of 12 pages can be used. The system supports non-blocking wire-speed switching via 24 10/100M ports.

8.13. Flow Control

The RTL8318P supports IEEE 802.3x full-duplex flow control, and half-duplex back pressure congestion control.

8.13.1. IEEE 802.3x Pause Flow Control

IEEE 802.3x flow control is auto-negotiated between the remote device and the RTL8318P by writing the flow control ability, via MDIO, to an external connected PHY.

If a good PAUSE frame is received from any PAUSE flow-control-enabled port with DA=0180C2000001, the corresponding port of the RTL8318P will stop its packet transmission until a PAUSE timer timeout, or another PAUSE frame with zero PAUSE time is received.

The maximum transmitted Pause frame count during a congestion event is controllable. (1) limited to a 128 count (2) unlimited count. The limited count is used to avoid unexpectedly long pause time locks for some network topology traffic.

This function is controlled by register 0x0001 [3].

Hardware Strapping Pin: MaxPauseCnt (79).

8.13.2. Half Duplex Back Pressure Flow Control

The RTL8318P supports two back pressure flow control schemes to force incoming packet backoff when the switch destination port is congested. This back pressure mode is controlled by register 0x0001 [7] and Hardware Strapping Pin: EnCOLBKPMode (119).

Collision-based back pressure: Uses a 4-byte jam pattern to force collisions with each incoming packet to force the link partner to back off transmissions according to CSMA/CD until the destination port congestion event is cleared. The RTL8318P uses a special half-duplex back pressure design; after 48 forced collisions it unconditionally receives and forwards one packet successfully. This prevents the connected repeater from being partitioned due to excessive collisions.

Carrier-sense-based back pressure: When a congested event is asserted, the RTL8318P continuously sends 4k jam packets with a minimum Inter-Packet Gap to prevent the link partner from transmitting more packets.

8.14. Broadcast Storm Filtering Control

The Broadcast Storm Filtering Control function enables each port to drop broadcast packets (Destination MAC ID is 'ff ff ff ff ff ff') after a ***continuous received broadcast packets counter*** count of 64. The counter is reset to 0 every 800ms or when receiving non-broadcast packets (Destination MAC ID is not 'ff ff ff ff ff ff').

This Broadcast Storm Filtering Control function is controlled by register 0x0607 [4].

Hardware Strapping Pin: EnBRDCTRL (11).

8.15. Head-Of-Line Blocking Prevention

The RTL8318P incorporates a simple mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. When the flow control function is disabled, the RTL8318P first checks the destination address of an incoming packet. If the destination port is congested, then the RTL8318P discards this packet to avoid blocking following packets destined for a non-congested port.

8.16. Port Trunking and Fault Recovery Support

Port Trunking is the ability to aggregate several 10/100Mbps ports into a single logical link. There are 4 trunk groups supported by the RTL8318P. They are identified as:

Trunk 0: (Port 0, 1, 2, 3)

Trunk 1: (Port 4, 5, 6, 7)

Trunk 2: (Port 8, 9, 10, 11)

Trunk 3: (Port 12, 13, 14, 15)

They are individually enabled by Register 0x0307[4:1], EnTrunk[3:0] during hardware reset. Each trunk supports a trunking port status LED. The LED will be active low when the trunking function is enabled.

The RTL8318P trunking port always sends packets over the same link path in the trunk with a given source and destination MAC address to prevent frames from getting out of order, but the reverse path may follow a different link.

8.16.1. Load Balancing

The load balancing scheme between links in a trunk group is determined by an Index[2:0] value that is calculated by a DA and SA hash algorithm.

Mapping algorithm. Given a number between 8 values of Index[2:0]:

If link up port is 4. Index value {(7, 6), (5, 4), (3, 2), (1, 0)} maps to LinkUpPort[3:0]

If link up port is 3. Index value {(7, 6, 5), (4, 3, 2), (1, 0)} maps to LinkUpPort[2:0]

If link up port is 2. Index value {(7, 6, 5, 4), (3, 2, 1, 0)} maps to LinkUpPort[1:0]

If link up port is 1. Index value {(7, 6, 5, 4, 3, 2, 1, 0)} maps to LinkUpPort[0]

8.16.2. Trunk Fault Auto Recovery

If a physical port of a trunk group is link down, then the EnTrunkLED will blink to warn of a link-down fault event. The Fault flag will be reported on register 0x0102 (System Fault Indication Register).

The RTL8318P will auto-start the Auto Fault Recovery scheme to distribute the trunk load to the remaining link up ports.

8.17. IGMP Snooping Support

The RTL8318P supports ASIC-based IGMP (Internet Group Management Protocol) snooping. This can be enabled via register 0x0308[0]. No other external CPU handling is required. It supports the ability to parse the IGMP control protocol packets and IP multicast data packets and learn the multicast router port and group address member ports into the multicast address table.

The RTL8318P differentiates between IGMP control protocol packets according to the message type:

- Router protocol packets (IGMP query packets and multicast routing protocol packets) are broadcast to all ports
- Group member protocol packets (IGMP v1, v2, Report and Leave packets) are sent directly to multicast router ports

IP multicast data packets involve multicast group table lookup and forwarding operations. If the table lookup returns a hit, the data packet is forwarded to all member ports and router ports. If the multicast address is not stored in the address table (i.e. lookup miss), the packet is broadcast to all ports of the broadcast domain.

The multicast table is combined with a L2 MAC table with a maximum of 8k entries. For a given multicast entry, the valid port member bit will auto age out after about 5 minutes if the port does not receive a corresponding group address IGMP report packet.

8.18. VLAN Function

The RTL8318P supports a VLAN function to segregate the switch into 32 VLANs. Each VLAN is a broadcast domain and each VLAN may be flexibly configured from 0 to 24 port members. Both port-based and tag-based VLAN functions are supported. The PVID, Tagging Control, and Ingress/Egress rules are manually configured on the VLAN Table at registers 0x030B~0x037C. The VLAN table format is shown as follows:

Table 14. VLAN Table Format

VLAN Entry Index	VID (12-Bit)	Port Member Set (26-bit Bitmap)
0		
1		
2		
:		
31		

'VID' defines the 802.1Q VLAN ID. The value of 'VID' may NOT be '0x000' or '0xfff'.

A VLAN is used to divide the broadcast domain to cut broadcast scope. The VLAN Frame Forwarding Rules are defined as follows:

- A received broadcast/multicast frame will be flood forwarded to VLAN member ports only ('Port Member Set' in the VLAN table) of the VLAN except the source port.
- A received unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded unless Leaky VLAN control is enabled.
- All VLAN groups share the same layer-2 learned MAC address table (Shared Learning).

8.18.1. Port-Based VLAN

By setting the 0x030B register to disable the En8021Qaware control bit, port-based VLAN is enabled and 802.1Q VLAN tagging is ignored. All other VLAN table configurations are the same as tag-based VLAN functions. The VLAN classification of an incoming packet on a port-based VLAN is defined by the port PVID. The RTL8318P uses the Port VLAN Identifier (PVID) to search the VLAN table for the VLAN member.

8.18.2. IEEE 802.1Q Tag-Based VLAN

By setting the 0x030B register to enable the En8021Qaware control bit, 802.1Q tag-based VLAN is enabled.

VLAN classification is the first step before VLAN table lookup. The method of assigning a unique VID value to a received packet is as follows:

1. For a VLAN-tagged packet.

   If the tagged 12-bit VID != 0, then the tagged VID value is used.

   If the tagged VID = 0 (Null VID, priority tag), then the port's PVID value is used.

2. For a non-VLAN-tagged packet, the port's 12-bit PVID value is used.

Note: The 'insert PVID' function for non-VLAN-tagged packets is controlled by registers 0x037D~0x037E).

After a unique 12-bit VID is assigned, the RTL8318P checks the VLAN table ingress/egress rule, and then forwards the packet to valid destination ports.

8.18.3. Ingress/Egress Filtering Control Parameters

Two VLAN filtering rule control parameters are provided on register 0x030B:

- Acceptable frame type control: Admits all frames or admits only VLAN-tagged frames
- Ingress filtering control: Enables filtering of frames received from a port that is not in this port's VLAN group

8.18.4. Leaky VLAN

The Leaky VLAN feature enables specific frames to be forwarded between different VLANs.

For example, if the VLAN table entry is:

VLAN 1: Port members = {Port 1, 2, 3}

VLAN 2: Port members = {Port 4, 5, 6}

Normally, broadcast, multicast, and unicast packets are not allowed to be switched between these two VLANs. Port 1 broadcast packets will only flood to Ports 2 and 3. A Port 1 unicast packet is not allowed to be forwarded to a member of VLAN 2.

If the Leaky VLAN function is enabled, three types of packets may be forwarded to destination ports outside the current VLAN.

- Unicast Packet: May be forwarded to a destination port (L2 table lookup hit) on a different VLAN
- ARP Broadcast Packet: May be broadcast to all ports on a switch
- IP Multicast Packet: May be flooded to all the multicast address group member set, ignoring the VLAN member set domain limitation

These types of leaky control are used when:

- A switch is divided into multiple VLANs and host to host communication is required between the different VLANs without using a router
- You want to improve router performance

8.18.5. Insert/Remove VLAN Priority Tag

The RTL8318P supports Output Priority tagging control via register set 0x0319~0x031B. There are four types of VLAN tagging:

1. Remove the VLAN tag from all tagged packets
2. Insert a priority tag into untagged high-priority packets (Set priority field: 7, VID field: 0 for high priority packets)
3. Insert a priority tag into all untagged packets
   (Set priority field: 7, VID field: 0 for high priority packet. Set priority field: 0, VID field: 0 for low priority packets)
4. Don't touch (No modification made to the packet)

Note: This function may be enabled whether the VLAN function is enabled or not.

8.19. QoS Function

The RTL8318P can recognize QoS priority information in an incoming packet and send the packet to different priority queues for different service priority. The RTL8318P identifies the packet's priority based on three types of QoS priority information:

- Port-based priority
- IEEE 802.1p/Q VLAN tag
- TCP/IP TOS/DiffServ (DS) priority field

These three types of QoS can be configured via hardware pins, EEPROM, or Registers 0x0400 ~ 0x0402.

The RTL8318P supports two priority level queues. The queue service rate is based on the Weighted Round Robin algorithm. The packet-based service weight ratio of high-priority and low-priority queuing can be set to 4:1, 8:1, 16:1 or 'Always high priority first'.

8.19.1. Port-Based Priority

When port-based priority is applied, any packet received from a high priority port will be treated as a high priority packet.

8.19.2. IEEE 802.1p/Q-Based Priority

When 802.1p tag priority is applied, the RTL8318P recognizes 802.1Q VLAN tagged packets and extracts the 3-bit User Priority information from the VLAN tag. The RTL8318P sets the User Priority threshold to 3. VLAN tagged packets with User Priority values 4~7 are treated as high priority packets, and other User Priority values (0~3) as low priority packets (follows the IEEE 802.1p standard).

8.19.3. Differentiated Services Based Priority

When TCP/IP's TOS/DiffServ (DS) based priority is applied, the RTL8318P recognizes TCP/IP Differentiated Services Codepoint (DSCP) priority information from the DS-field defined in RFC2474. The DS field byte for IPv4 is the Type-of-Service (TOS) octet. Recommended DiffServ Codepoints are defined in RFC2597 for classifying traffic into different service classes. The RTL8318P extracts the codepoint value of the DS field from IPv4 packets and identifies the priority of the incoming IP packet following the definitions listed below:

High Priority. DS-field = 101110 (EF, Expected Forwarding)

001010; 010010; 011010; 100010 (AF, Assured Forwarding)

11x000 (Network Control)

Low Priority. DS-field = Other values

VLAN tagged packet formats are shown below:

6 bytes	6 bytes	2 bytes	3 bits	1 bit	12 bits		4 bytes
DA	SA	81-00	User Priority (0~3: Low-pri; 4~7: High-pri)	CFI	VLAN Identifier	Data	CRC

Figure 5. 802.1Q VLAN Tag Frame Format

6 bytes	6 bytes	4 bytes	2 bytes	4 bits	4 bits	6 bits	2 bits		4 bytes
DA	SA	802.1Q Tag (Optional)	08-00	Version IPv4: 0100	IHL	TOS[0:5]: DS-field	----	Data	CRC

Figure 6. IPv4 Frame Format

8.19.4. Flow Control Auto Turn Off

The RTL8318P can automatically turn off IEEE 802.3x flow control and back pressure flow control for 1~2 seconds whenever the port receives a high priority packet. Flow control is re-enabled when no priority packets are received for 1~2 seconds. This auto-turn off function is enabled via Register 0x0400[2].

8.20. Ingress and Egress Bandwidth Control

The RTL8318P supports bandwidth control on all ports. Each port's bandwidth is configurable on both ingress and egress traffic independently. Port bandwidth may be configured to 128kbps, 256kbps, 512kbps, 1Mbps, 2Mbps, 4Mbps, or 8Mbps.

When the ingress or egress traffic bandwidth exceeds the configured threshold, flow control is triggered to limit the throughput. The control description is shown in register 0x020A ~0x0211, 0x0215.

8.21. Simple MIB Counter Support

Three 32-bit MIB counters (Counter 1, Counter 2, and Counter 3) are implemented on each port for basic traffic management and diagnostic purposes.

The MIB object of each counter is configurable. The MIB object selection on each counter is shown in Table 15. A detailed description is given in 10.8 MIB Counter Register, page 62.

Table 15. MIB Object Selection

MIB Object	Counter 1	Counter 2	Counter 3
RX Packet Count	V	-	-
RX Byte Count	V	-	-
TX Packet Count	-	V	-
TX Byte Count	-	V	-
Drop Packet Count	-	-	V
Drop Byte Count	-	-	V
CRC Error Packet Count	V	V	V
Collision Count	V	V	V

8.22. Realtek Remote Control Protocol

The Realtek Remote Control Protocol (RRCP®) is a Realtek proprietary simple and easy device management program that is implemented for in-band remote control purposes.

The protocol is hardware ASIC-based and does not require an external CPU. It allows the system administrator to get/set the switch configuration, to read the statistic counters, and to find RRCP aware devices.

The Remote Management Tool (RMT) software package is bundled with the RTL8318P. The RMT is a Windows-based tool developed to enhance the functionality of Realtek's dumb layer 2 switches via software. The RMT gives network administrators the ability to remotely configure and monitor dumb layer 2 switches as though they were intelligent switches.

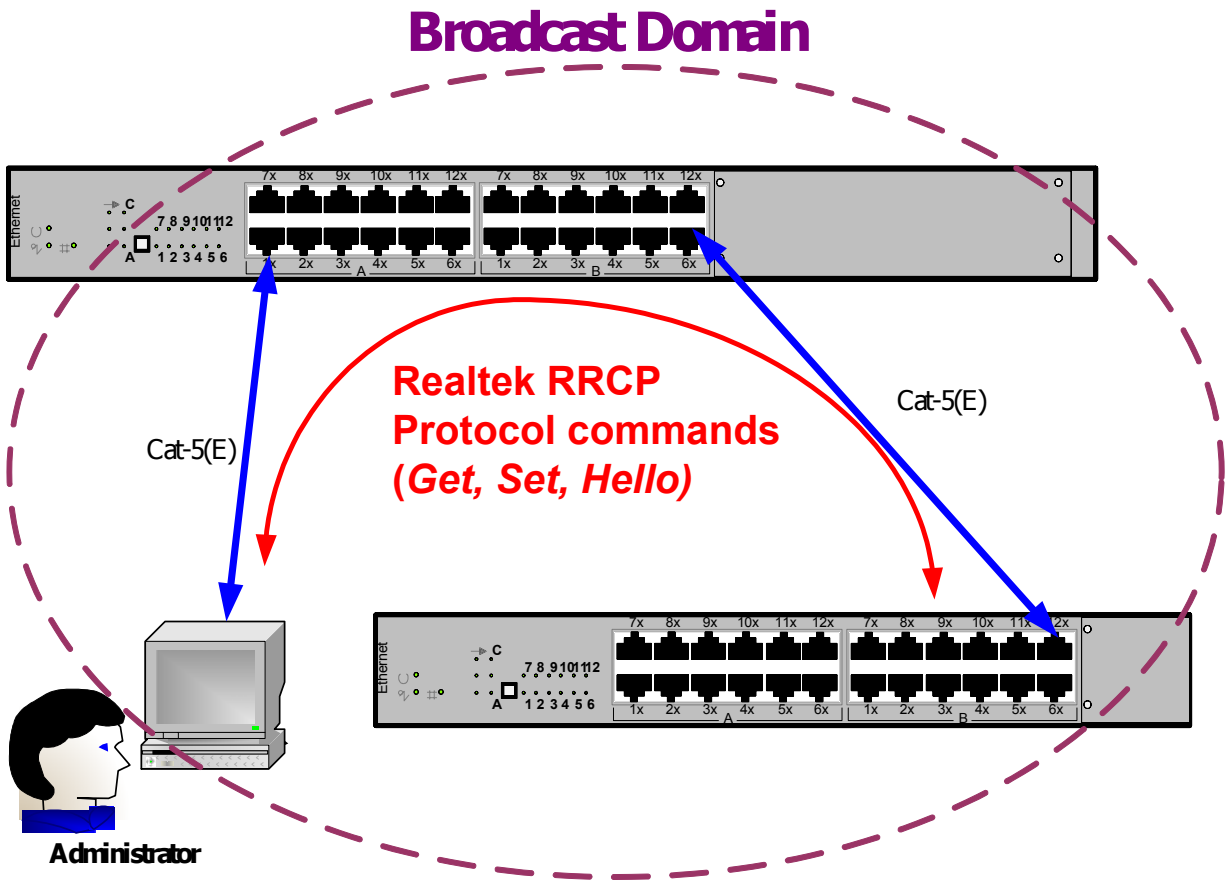


Figure 7. Realtek Remote Control Protocol

8.22.1. RRCP® Capabilities

The RRCP is limited to the same network domain.

The RRCP supports the following:

1. Network Topology Discovery
2. Get/Set Configuration value of Register
3. Security Management by an Authentication Key and management port setting

Operation commands are:

Management Operation (1) register Get
(2) register Set
(3) Hello

Switch Operation (1) register Get Reply
(2) Hello Reply

The Hello Reply packet reports the switch's link vector information back to the manager (Downlink MAC, Downlink Port), (Uplink MAC, Uplink Port). The link vector information enables discovery of the network topology.

8.22.2. Management Security Scheme

Two RRCP security schemes are implemented:

RRCP Management Authorized Port Control

An authorized port can be configured via registers 0x0201~0x0202. Only RRCP packets originating from an authorized port will be processed and responded to. Other RRCP with DA=switch's MAC address will be dropped.

Protocol Authentication Key control

Each RRCP packet must contain the Authentication Key defined in the register 0x0209. After powering on, the Authentication Key is reset to the default value (0x2379). It can be updated through a valid RRCP Set command or through a Serial CPU interface.

8.22.3. RRCP® Protocol Packet Format

Hello/Get/Set/Get_Reply Packet Format

Table 16. Hello/Get/Set/Get_Reply Packet Format

0	8	16	24 ~ 32
DA (6)			
DA		SA (6)	
SA			
RealtekEtherType (2)		Protocol (1)	r OP Code (7bit)
Authentication Key (2)		Register Address (2)	
Register Data (4)			
Reserved (4)			
Reserved (4)			
Pad 00 : :			
CRC (4)			

Hello/Get/Set/Get_Reply Packet Format Description

Table 17. Hello/Get/Set/Get_Reply Packet Format Description

Field	Length	Description	Value
DA	6B	Destination MAC Address. -For a Get, Set packet, this is the unicast address of a switch. -For a Get_Reply packet, this is the unicast address of the management station. -For a Hello packet, this can be the unicast address of a switch or a broadcast address to all RRCP aware switches. Note: If the Authentication Key register has been updated after power on, the switch will only respond to a unicast Hello packet.	--
SA	6B	Source MAC address.	--
RealtekEtherType	2B	Identifies the packet as a Realtek Remote Control packet. The EtherType value=0x8899.	0x8899
Protocol	1B	Realtek Proprietary protocol type definition. 01: Realtek Remote Control Protocol Others: Reserved	01h
OP Code	7bit	Operation Code (7bit). Code definition: 00: Hello packet 01: Get configuration 02: Set configuration	--

Field	Length	Description	Value
r	1 bit	Reply flag. On receiving a control packet reply from the switch to the management station, this flag will be set to 1. Otherwise, this bit should be 0.	Station to switch: 0 Switch to station: 1
Authentication Key	2B	Authentication Key. Used for security of the management operation. The Key value can be modified by the administrator via a remote control packet. A received control packet with a valid Destination MAC address but with an unmatched authentication key will be dropped with no reply. If the DA is a broadcast address or is the address of another switch, it will still be relayed.	Default: 0x2379
Register Address	2B	Register address of the configuration.	--
Register Data	4B	Register data of the configuration.	--

Hello_Reply Packet Format

Table 18. Hello_Reply Packet Format

0	8	16	24 ~ 32
DA (6)			
DA		SA (6)	
SA (=Downlink MAC)			
RealtekEtherType (2)		Protocol (1)	r OP Code (7bit)
Authentication Key (2)		Downlink Port (1)	Uplink Port (1)
Uplink MAC (6)			
Uplink MAC		Chip ID (2)	
Vender ID (4)			
Pad 00 : :			
CRC (4)			

Hello_Reply Packet Format Description

Table 19. Hello_Reply Packet Format Description

Field	Length	Description	Default
Downlink Port	1B	Downlink Port number of the link vector. Indicates the port number on the Hello Reply switch that is connected to the Uplink switch. This is set by the Hello reply switch.	--
Uplink Port	1B	Uplink Port number of the link vector. Indicates the port number of the Uplink switch that is connected to the Hello reply switch. This is set by the Uplink switch.	00h Updated by the Uplink_MAC switch
Uplink MAC	6B	The MAC address of the Uplink switch. The default value is 000000000000h and is updated by the Uplink switch. When a switch receives a Hello_Reply frame with zero UplinkMAC, then it will enter the SA MAC address here.	0
Chip ID	2B	Realtek Chip ID. This is set by the Hello_Reply switch. Each Realtek switch controller that is aware of the RRCP has a unique Chip ID (see 11.3.7 0x0206H: Chip Model ID, page 72).	EEPROM
Vender ID	4B	Vender ID. This is set by the Hello_Reply switch. The 4-byte vender ID is reserved for the system vender to configure its company name or the device model ID.	EEPROM

8.23. Network Loop Connection Fault Detection

The RTL8318P periodically transmits a Realtek-EtherType (=0x8899) protocol frame to detect network loop faults.

- Normal transmission time interval is five minutes
- If a port detects a loop, the loop event flag will be set (register 0x0101) and the transmission time interval will change to one second to speed up the new topology change detection
- The loop event flag will be cleared and the transmission time interval will return to five minutes if the port does not receive a self-loop detect packet for 3 seconds

Loop Detect Packet Format

The Loop Detect Packet Format is shown below:

Table 20. Loop Detect Packet Format

0	8	16	24 ~ 32
DA (6) [=0xffffffffffff]			
DA		SA (6)[=Switch MAC]	
SA			
RealtekEtherType (2) [=0x8899]		Protocol (1) [=03]	Pad 0000
Pad 00000000 : :			
CRC (4)			

8.24. Realtek Echo Protocol

The Realtek Echo Protocol (REP) supports the Layer 2 Echo test. It is easy for a host to do network connection diagnostics through a simple test packet, with or without other hosts on the network. No IP assignment is required.

When the RTL8318P receives a REP packet, it replies by sending the original REP frame to the source MAC address with the DA and SA exchanged.

Realtek Echo Protocol Frame

The REP frame format is shown below:

0	8	16	24 ~ 32
DA (6) [=0xffffffffffff]			
DA		SA (6)[=Switch MAC]	
SA			
RealtekEtherType (2) [=0x8899]		Protocol (1) [=02]	Pad 0000
Pad 00000000 : :			
CRC (4)			

Figure 8. Realtek Echo Protocol Frame

8.25. Disable Port

A port can be disabled via the Port Disable Control Register (register 0x0608~0x0609). When a port is disabled, the port will cease all packet transmission and reception except for Realtek Remote Control Protocol (RRCP) packets. The physical link status is not changed.

8.26. Port Properties Configuration

The RTL8318P supports a flexible method to configure port properties via the PHY MII registers. Configurable properties include Media Speed (10M/100M), Duplex Mode, and 802.3x PAUSE flow control. The properties of each can be configured by auto-negotiation or forced mode (auto negotiation disabled).

The port link state will be reported in the port Link Status registers. The configuration description is shown in registers 0x060A ~ 0x0624.

Gigabit Port Pause Ability configuration is as follows:

Table 21. Gigabit Port Pause

Local Device Setup (DUT)		Link Partner Setup (Testing Device)		Target Resolution	
PAUSE (1000Base-X: Reg4.7) or (1000Base-T: Reg4.10)	ASM_DIR (1000Base-X: Reg4.8) or (1000Base-T: Reg4.11)	PAUSE (1000Base-X: Reg5.7) or (1000Base-T: Reg5.10)	ASM_DIR (1000Base-X: Reg5.8) or (1000Base-T: Reg5.11)	Local Resolution (DUT)	Link Partner Resolution (Testing Device)
1 ◄──►	-	1	-	Enable PAUSE TX/RX	Enable PAUSE TX/RX
1	1	0	1	Enable PAUSE RX ◄	Enable PAUSE TX
0	1	1	1	Enable PAUSE TX ►	Enable PAUSE RX
Others		Others		Disable PAUSE	Disable PAUSE

The following shows how to configure the Pause and Asymmetric Pause ability on port property registers (0x060A~0x0615) to get an expected negotiation result.

Table 22. Configuring Pause and Asymmetric Pause

PAUSE	Asymmetric PAUSE	Expected PAUSE Result
0	0	Disable
0	1	Asymmetric to Link Partner
1	0	Symmetric
1	1	Asymmetric to Link Local or Symmetric

When a port is configured to 'Forced Mode' (auto negotiation disabled), the following table shows how to configure flow control ability (TX pause/RX pause) on port property registers (0x060A~0x0615) to get an expected negotiation result.

Table 23. TX/RX Pause Ability in Forced Mode

(0x060A~0x0615) bit[6] Asymmetric PAUSE	(0x060A~0x0615) bit[5] Asymmetric PAUSE	RTL8318P Flow Control Ability
0	0	RX pause ability only
0	1	No Flow Control ability
1	0	TX pause ability only
1	1	Both TX/RX pause ability

8.27. Serial CPU Interface

The RTL8318P supports a serial CPU interface (Slave mode) that shares the same hardware pin (SCK, SDA) as the EEPROM interface (Master mode). The EEPROM and Serial interface can coexist by assigning a different device ID. Define EEPROM device ID=1010-000, RTL8318P device ID=1010-100. The interface is compatible with EEPROM 24LC08.

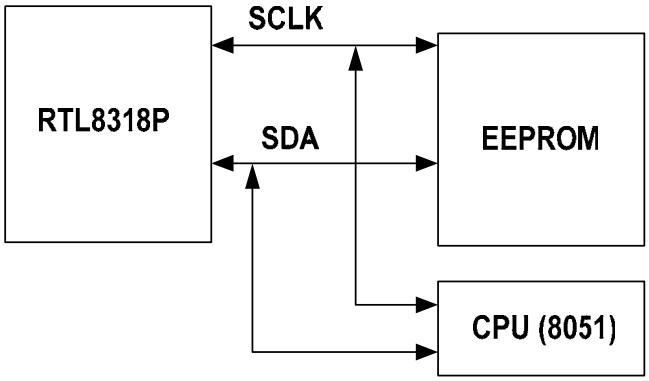


Figure 9. Serial CPU Interface

The serial CPU interface is enabled after the EEPROM download has finished. When operating in serial CPU mode the SCK is an input pin. The SDA is an IO pin with internal pull high.

8.27.1. Serial-CPU Access Format

In Serial CPU mode, 16-bit and 32-bit data access are both supported by the RTL8318P. The Serial Read Write access format is as follows.

- 16-bit Address (MSB first)
- 16/32-bit data Burst Read (Low byte (Byte0) first; MSB first)
- 16/32-bit data Burst Write (Low byte (Byte0) first; MSB first)

Note: Each burst is one byte.

Start and Stop Definition (START; STOP)

A high-to-low transition of SDA with SCLK high is a START condition and it must precede any other command.

A low-to-high transition of the SDA line while the clock (SCLK) is HIGH determines a STOP condition. All operations must end with a STOP.

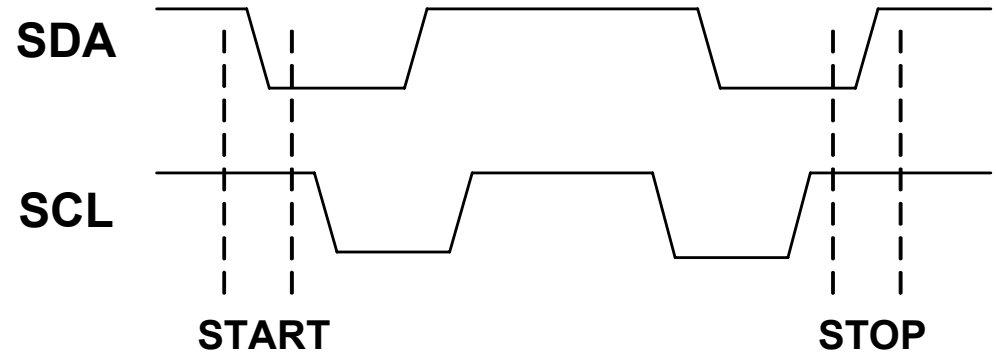


Figure 10. Start and Stop Definition

Output Acknowledge (ACK)

When addressed, each receiving device is obliged to generate an acknowledgment after reception of each byte.

The master device must generate an extra clock pulse that is associated with this acknowledgement bit.

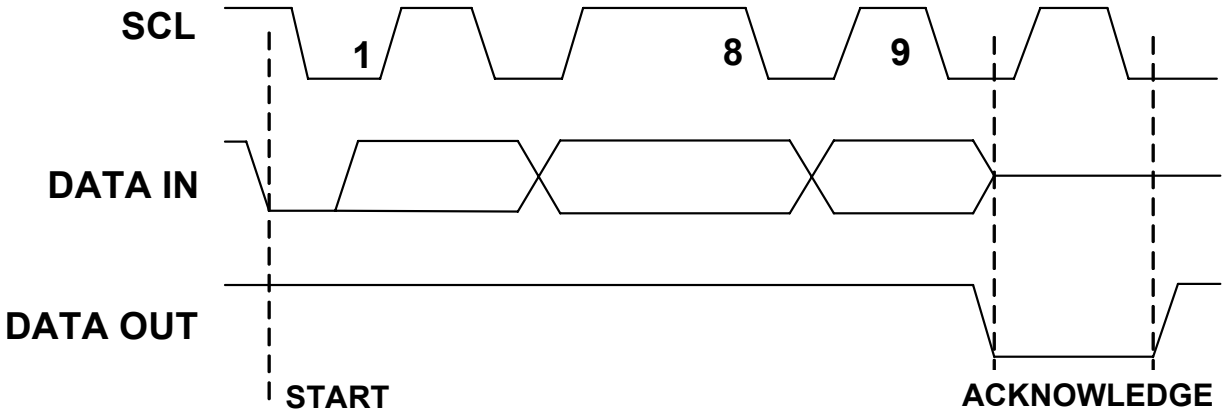


Figure 11. Output Acknowledge (ACK)

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal.

The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Serial CPU 16-Bit Read/Write Format

Table 24. Serial CPU 16-Bit Read/Write Format

Bit Width	1	4	3	1	1	8	1	8	1	8	1	8	1	1
Operation	Start Bit	Control code	Chip Select	RW	Ack	Reg. Addr. [7:0] (MSB first)	Ack	Reg. Addr. [15:8] (MSB first)	Ack	Reg. Data. [7:0] (MSB first)	Ack	Reg. Data [15:8] (MSB first)	Ack	Stop Bit
16-bit Read	Start	1010	100	1	0 (*A)	Write Data	0 (*A)	Write Data	0 (*A)	Read Data	0 (*B)	Read Data	1 (*B)	Stop
16-bit Write	Start	1010	100	0	0 (*A)	Write Data	0 (*A)	Write Data	0 (*A)	Write Data	0 (*A)	Write Data	1 (*A)	Stop

*Note: *A = ACK by RTL8318P. *B = ACK by CPU*

Serial CPU 32-Bit Read Format

Table 25. Serial CPU 32-Bit Read Format

Bit Width	1	4	3	1	1	8	1	8	1	8	1	8	1	8	1	8	1	1
Operat-ion	Start Bit	Control code	Chip Select	RW	Ack	Reg. Addr. [7:0] (MSB first)	Ack	Reg. Addr. [15:8] (MSB first)	Ack	Reg. Data. [7:0] (MSB first)	Ack	Reg. Data. [15:8] (MSB first)	Ack	Reg. Data. [23:16] (MSB first)	Ack	Reg. Data [31:24] (MSB first)	Ack	Stop Bit
32-bit Read	Start	1010	100	1	0 (*A)	Write Data	0 (*A)	Write Data	0 (*A)	Read Data	0 (*B)	Read Data	0 (*B)	Read Data	0 (*B)	Read Data	1 (*B)	Stop

*Note: *A = ACK by RTL8318P. *B = ACK by CPU.*

8.27.2. EEPROM RW Command Format

The RTL8318P provides a self-Read/Write EEPROM function, which can save and recall user configuration via the Realtek Remote Management Tool (RMT). Read/Write EEPROM function control is via register 0x0217~0x0218.

Table 26. 0x0217H: EEPROM RW Command Register

Bits	Name	Description	RW	Default
7:0	EEPROM Address	Assigns EEPROM address bits	RW	0
10:8	CHIP_SEL[2:0]]	Assigns chip selection bits	RW	0
11	Read/Write Operation	0: Write Operation 1: Read Operation	RW	0
12	Status	0: Idle 1: Busy	RW	0
13	Operation Success status	0: Operation Succeeded 1: Operation Failed (Read to Clear)	RW	0
15:14	Reserved			

Table 27. 0x0218H: EEPROM RW Data Register

Bits	Name	Description	RW	Default
7:0	WdataEE[7:0]	Data to be written to EEPROM	RW	0
15:8	RdataEE[15:8]	Data Read from EEPROM	R	0

EEPROM Read/Write Procedure

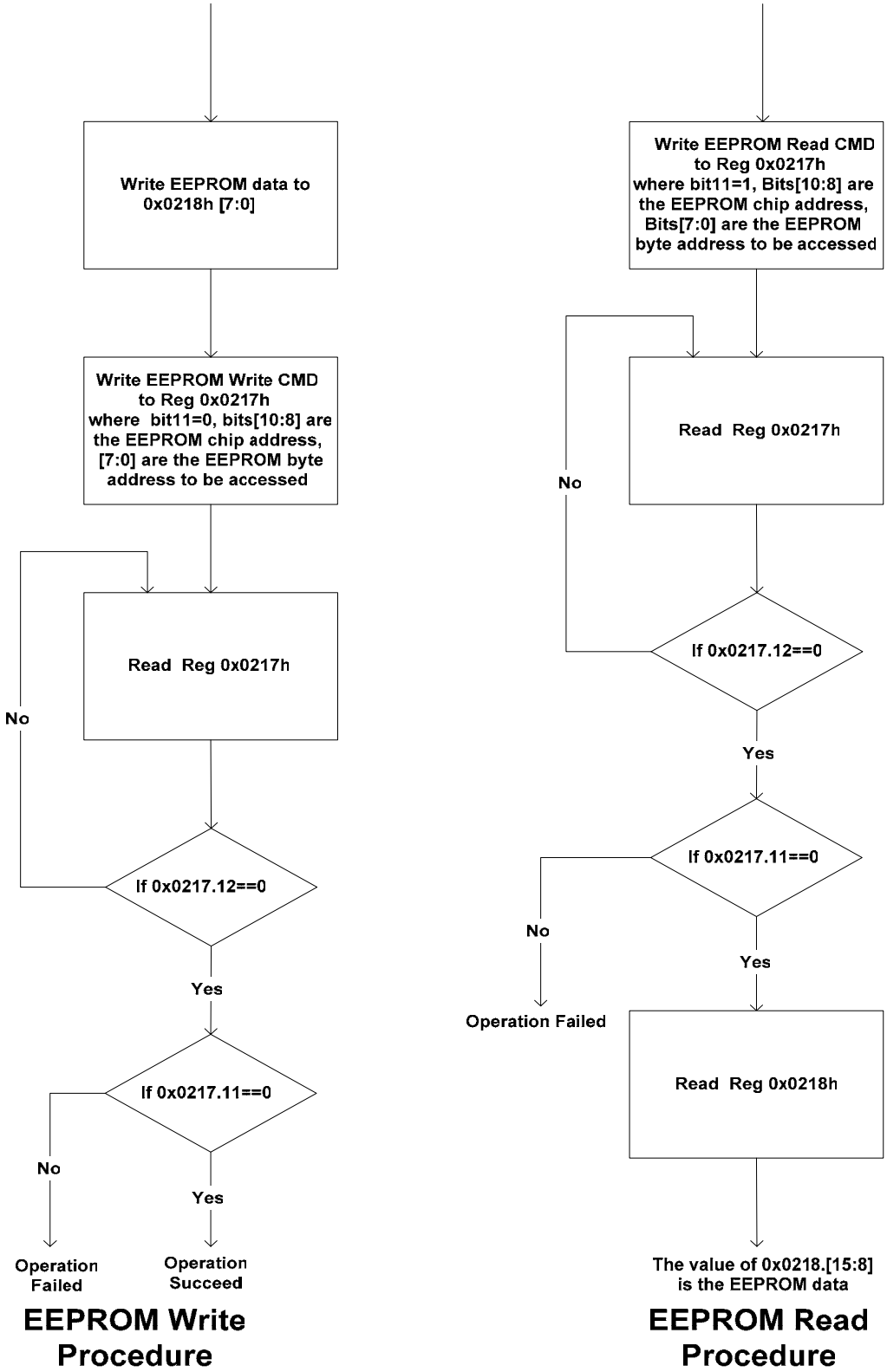


Figure 12. EEPROM Read/Write Procedure

8.28. PHY Serial Management Interface

The RTL8318P supports PHY management through the serial MDIO and MDC signal (SMI) to start the auto-negotiation process. After a power-on reset, the RTL8318P writes its abilities to the advertisement registers 0, and 4 of the connected PHY and commands the PHY to restart the auto negotiation process. The PHY device address setting is defined as:

- Address 16~31 for Fast Ethernet ports 0~15
- Address 2 for Gigabit port
- Address 5 for MII port

After restarting auto-negotiation, the RTL8318P will continuously read the link status and abilities of local and link partners to determine the link state.

Port properties (speed, duplex, 802.3x flow control) can be configured via auto-negotiation or forced mode. The configuration is described in register 0x060A ~ 0x0615. The final link status is reported in register 0x0619~0x0624.

8.28.1. SMI (MDC, MDIO) Interface

SMI (MDC, MDIO) Management Packet Format

Table 28. SMI (MDC, MDIO) Management Packet Format

	Management Frame Fields							
	PRE	**ST**	**OP**	**PHYAD**	**REGAD**	**TA**	**DATA**	**IDLE**
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

8.28.2. PHY Register Indirect Access

The RTL8318P supports the ability to randomly access PHY registers through a set of control registers at 0x0500~0x0502. Users need to define the PHY address ID, PHY Register ID, Data content of the write command, and operating command type (Read or Write) on the above registers. Then the RTL8318P will auto process the PHY Read/Write access through the MDC/MDIO interface.

Read PHY Register Procedure

- Configure PHY Access Control Register (0x0500)
- Read the result on PHY Access Read Data Register (0x0502)

Write PHY Register Procedure

- Write the PHY Access Write Data Register (0x0501)
- Configure the PHY Access Control Register (0x0500)

PHY Address ID Definition

The PHY address ID corresponds to the port location. The PHY address ID of Ports 0~15 are 0x10, 0x11, 0x12 …., 0x1F, gigabit port is 0x02, and MII port is 0x05.

8.29. LED Interfaces

The RTL8318P provides a flexible per-port LED display to show the first 17 ports link status and diagnostic information. Both a parallel and serial interface are provided to drive the LEDs.

During power on reset, the parallel LED signals are driven low and the serial interface shifts to a low value for about two seconds to turn on all the LEDs for testing purposes.

8.29.1. Parallel LED Interface

The parallel interface only provides a system status LED.

LED signals include: LED_loopDet, LED_EnTrunk[5:0].

8.29.2. Serial LED Interface

Note: The serial LED interface is disabled when using MII mode.

The serial interface, SLED_CLK, and SLED_DATA provide clock and data to enable the external shift registers 74164 to capture the per-port link status and diagnostic information.

Another pin, LED_DMODE_CLK, provides the diagnostic items selection control. Each pulse signal input from this pin changes the diagnostic item to be displayed on the diagnostic LED.

Each port provides three port-state LEDs (StateLED) and one diagnostic LED (DiagLED). The LED display type can be flexibly configured and can be enabled or disabled to achieve the optimal BOM cost.

The LED display configuration is controlled by register 0x0005h 'LED Display Configuration Register', and can also be configured via EEPROM.

The StateLED display is defined by StatLED_mode[2:0] on register 0x0005. The available display types are shown in the following table.

Table 29. Serial LED Interface

StatLEDn_mode[2:0]	000	001	010	011	100	101	110	111
StateLEDn Display Type	Link /Act	100Spd	Duplex /Col	Link/Act /100Spd	Duplex	Act	Link	Col

The display items of the diagnostic LED (DiagLED) are internally defined and are as follows:

Table 30. Diagnostic LED Display

Item	Description
(DiagItem_0) DisablePort/RxError	ON: Disabled port Blinking: RX CRC error
(DiagItem_1) FlowControl/FCActive	ON: Flow control enabled Blinking: Flow control active
(DiagItem_2) TrunkPort/TKFault	ON: Trunking enabled port Blinking: Trunk fault warning
(DiagItem_3) HighPriorityPort	ON: High priority port
(DiagItem_4) LoopDetectPort	ON: Network loop connection fault detect
(DiagItem_5) BroadcastStormAlarmPort	ON: Broadcast Storm Alarm port
(DiagItem_6) NULL	Reserved
(DiagItem_7) NULL	Reserved

The DiagLED display item is changed by a trigger signal input from hardware pin 'LED_DMODE_CK'. The change sequence order of the DiagLED is:

DiagItem_0 → DiagItem_1→ DiagItem_2→ ……. → DiagItem_7→ Loop to DiagItem_0

8.29.3. Serial LED Display Panel Example (4 LEDs, Register 0x0005)

Enable Serial LED Display Mode:

➔ set EnSerialMode: 1

Define Per-port 4 LED Display Mode:

➔ Configuration. set EnLED[3:0]: 1111

Define the statLED display type as: StatLED0=Link/Act, StatLED1=10/100M, StatLED2=Duplex/Collision:

➔ Configuration. set StatLED0_mode[2:0]=000, StatLED1_mode[2:0]=001, StatLED2_mode[2:0]=010

Follow the same method to configure the per-port 1 LED, per-port 2 LED, and per-port 3 LED display mode, with or without enabling the diagnostic LED.

The LED panel is shown in Figure 13.

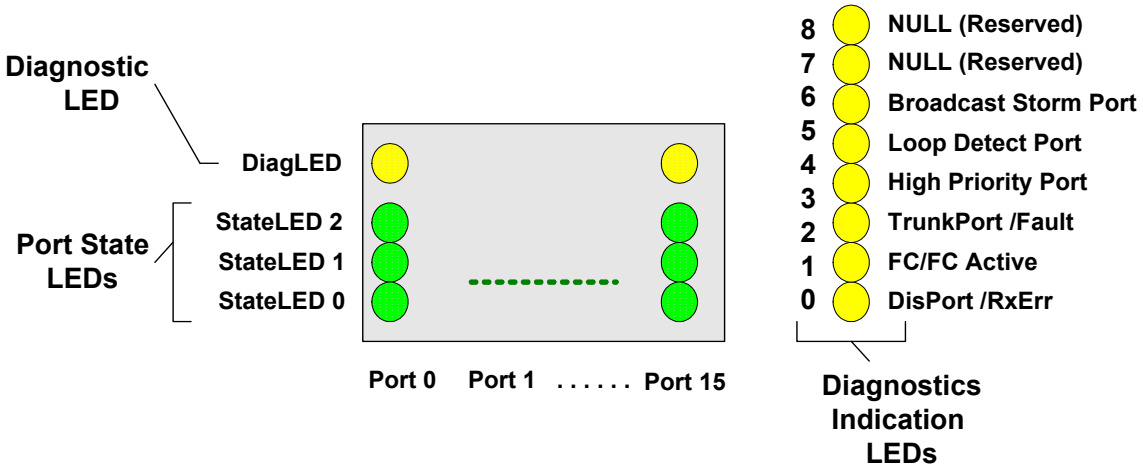


Figure 13. Serial LED Display

8.29.4. Serial LED Shift Out Sequence Order

The Serial LED output sequence is defined as follows: (first bit →….→ last bit).

Each port has four LEDs. There are eight diagnostic LEDs:

→ [P0 StateLED0] → [P0 StateLED1] → [P0 StateLED2] → [P0 DiagLED0]
→ [P1 StateLED0] → [P1 StateLED1] → [P1 StateLED2] → [P1 DiagLED0]
→- - - - - - - - - - - - →- - - - - - - - - - - - →- - - - - - - - - - - - →- - - - - - - - - - - -
→ [P15 StateLED0] → [P15 StateLED1] →[P15 StateLED2] → [P15 DiagLED0]
→ [Reserved_(DiagS0)] → [Reserved_(DiagS1)] → [Reserved_(DiagS2)] → [Reserved_(DiagS3)]
→ [Reserved_(DiagS4)] → [Reserved_(DiagS5)] → [Reserved_(DiagS6)] → [Reserved_(DiagS7)]

8.29.5. SCAN LED Interface

The RTL8318P supports Scan LED display mode. The forms of LED status streams, as shown below, are controlled by HW pin LEDMODE[1:0] = 2b'00 , and are latched upon reset.

Table 31. Scan LED Status

LED Status	Description
Spd	Speed Indicator High for 100Mbps and low for 10Mbps
Link/Act	Link, Activity Indicator High for link established Blinks when the corresponding port is transmitting or receiving
Col/Fulldup	Full duplex, Collision Indicator High for full duplex, and low for half duplex mode Blinks when there are collisions on the corresponding port

The RTL8318P provides three Scan LED groups that display each port's status:

Group A
(Scan_LEDA[5:0], Scan_STSA[3:0]) displays status for port0~port7

Group B
(Scan_LEDB[5:0], Scan_STSB[3:0]) displays status for port8~port15

Scan_LEDA[5:0], Scan_LEDB[5:0] operate with the same timing phase. The Scan LED timing diagram is shown below:

Scan LED Timing Diagram

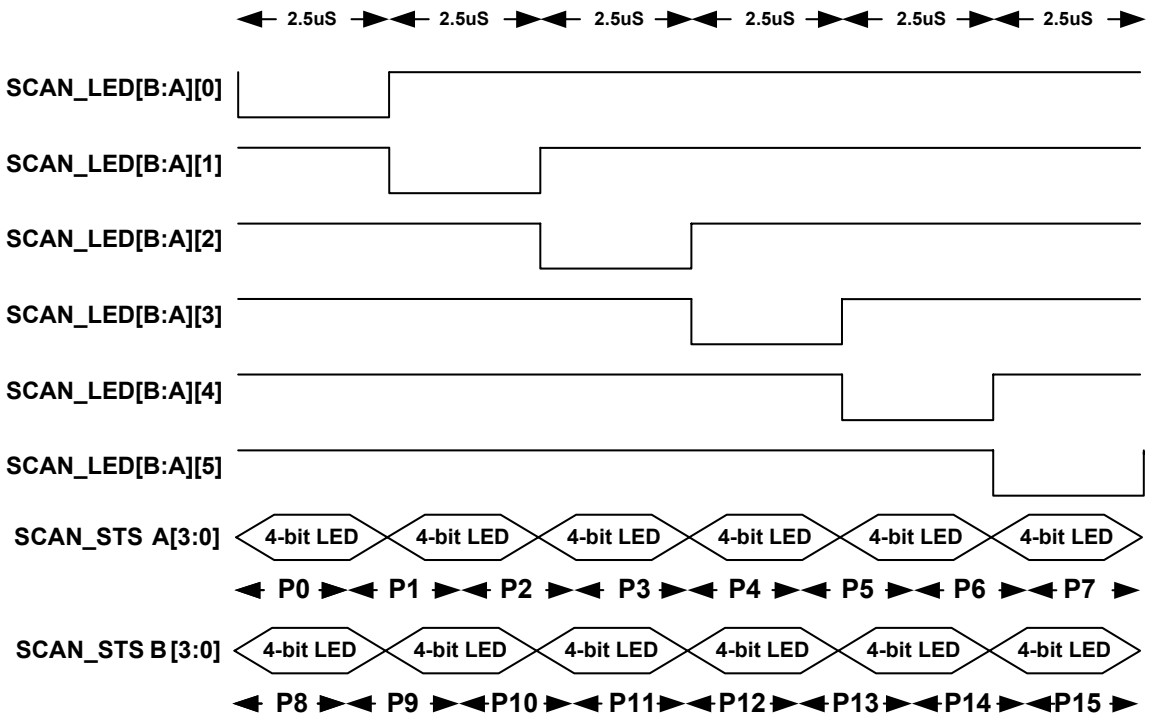


Figure 14. Scan LED Timing Diagram

External Circuit for Scan LED

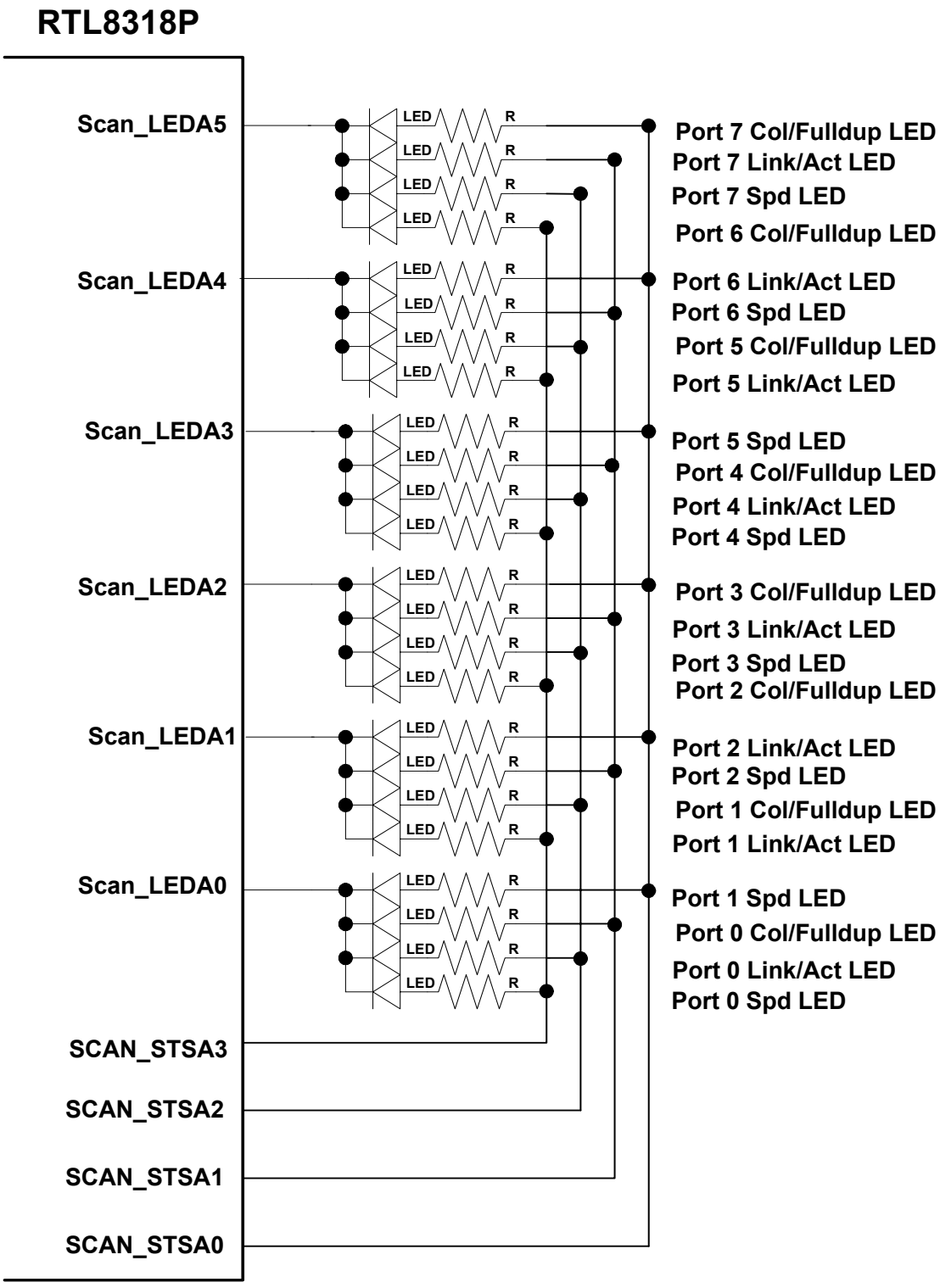


Figure 15. External Circuit for Scan LED

8.30. Port Mirroring

Port mirroring is used to forward traffic to a selected port based on one or more of the following:

- All traffic received from one or multi selected source ports (source mirroring)
- All traffic transmitted to one selected destination port (destination mirroring)

Table 32. Port Mirror Control Register for P15-P0, Gigabit Port, MII port

Register	Bits	Name	Description	RW	Default
0x0219	15:0	EnPortMirror(0)[15:0]	Enables the port-based mirror function. Bit n corresponds to port n. Write '1' to enable a port's mirror function	RW	0
0x021A	7:6	EnPortMirror(1)[7:6]	Enables the port-based mirror function. Write '1' to enable a port's mirror function Bit [6]: Gigabit Port control bit Bit [7]: MII Port control bit	RW	0

Table 33. RX Mirror Port Register for P15-P0, Gigabit Port, MII port

Register	Bits	Name	Description	RW	Default
0x021B	15:0	Mirror_RX(0)[15:0]	Bit n corresponds to port n. Write '1' to duplicate port n RX data to mirrored port.	RW	0
0x021C	7:0	Mirror_RX(1)[7:0]	Bit [6]: Gigabit Port control bit Bit [7]: MII Port control bit Write '1' to duplicate port n RX data to mirrored port.	RW	0

Table 34. TX Mirror Port Register for P15-P0, Gigabit Port, MII port

Register	Bits	Name	Description	RW	Default
0x021D	15:0	Mirror_TX(0)[15:0]	Bit n corresponds to port n. Write '1' to duplicate port n TX data to mirrored port.	RW	0
0x021E	7:0	Mirror_TX(1)[7:0]	Bit [6]: Gigabit Port control bit Bit [7]: MII Port control bit Write '1' to duplicate port n TX data to mirrored port.	RW	0

9. Serial EEPROM Configuration (24LC08)

The EEPROM configuration bits are directly mapped to some of the internal registers. For example, EEPROM addresses 0x00h and 0x01h directly map to internal register 0x0002 'RX IO PAD Delay Configuration'.

The mapping rule is: EEPROM 0x00h: REG. 0x0002[7:0], EEPROM 0x01h: REG. 0x0002[15:8].

9.1. EEPROM Configuration vs. Internal Register Mapping

Table 35. EEPROM Configuration vs. Internal Register Mapping

EEPROM Physical Address (8-Bit Data Entry) (24LC08)	Description	Corresponding Internal Register Address Mapping	Internal Default
01~00	Internal Use	0x0002	0A80
03~02	Reserved		
05~04	LED Display Configuration 0	0x0005	0E88
07~06	LED Display Configuration 1	0x0006	--
09~08	Reserved		
0B~0A	Reserved		
0D~0C	Realtek Protocol Control	0x0200	0000
0F~0E	RRCP security Mask Configuration 0	0x0201	0000
11~10	RRCP security Mask Configuration 1	0x0202	0000
13~12	Switch MAC ID 0	0x0203	0000
15~14	Switch MAC ID 1	0x0204	0000
17~16	Switch MAC ID 2	0x0205	0000
19~18	Chip ID 0	0x0206	0000
1B~1A	Vender ID 0	0x0207	0000
1D~1C	Vender ID 1	0x0208	0000
1F~1E	Reserved		
21~20	Reserved		
23~22	ALT Configuration	0x0300	0004
25~24	Port Trunking Configuration	0x0307	0000
27~26	IGMP Control Register	0x0308	0000
29~28	VLAN Control Register	0x030B	0000
2B~2A	Reserved		
2D~2C	Reserved		
2F~2E	QoS Control Register	0x0400	0010
31~30	Port Priority Configuration 0	0x0401	0000
33~32	Port Priority Configuration 1	0x0402	0000
35~34	Reserved		
37~36	Reserved		
39~38	Global Port Control Register	0x0607	0010
3B~3A	Port property Configuration 0	0x060A	AFAF
3D~3C	Port property Configuration 1	0x060B	AFAF
3F~3E	Port property Configuration 2	0x060C	AFAF

EEPROM Physical Address (8-Bit Data Entry) (24LC08)	Description	Corresponding Internal Register Address Mapping	Internal Default
41~40	Port property Configuration 3	0x060D	AFAF
43~42	Port property Configuration 4	0x060E	AFAF
45~44	Port property Configuration 5	0x060F	AFAF
47~46	Port property Configuration 6	0x0610	AFAF
49~48	Port property Configuration 7	0x0611	AFAF
4B~4A	Reserved		
4D~4C	Reserved		
4F~4E	Reserved		
51~50	Port property Configuration 8	0x0615	AFAF
53~52	Internal use	0x0616	--
55~54	Reserved		
57~56	Reserved		
59 ~~~ 5F	Reserved		
61~60	Designer Diagnostic Configuration	0xFFFF	0000
63~62	Reserved		
63~62	Reserved		
65~64	Reserved		
67~66	Reserved		
69~68	Port Disable Port0~Port15	0x0608	0000
6B~6A	Port Disable Gigabit Port and MII Port	0x0609	0000
6D~6C	Reserved		
6F~6E	Reserved		
71~70	RRCP Password	0x0209	2379
73~72	Port Mirror Control Register for P15~P0	0x0219	0000
75~74	Port Mirror Control Register for MII and Gigabit Port	X	
77~76	RX Mirror port mask for P15~P0	0x021B	0000
79~78	RX Mirror port mask for MII and Gigabit Port	X	
7B~7A	TX Mirror port mask for P15~P0	0x021D	0000
7D~7C	TX Mirror port mask for MII and Gigabit Port	X	
7F~7E	Reserved		
81~80	BW Control Register for P01~P00	0x020A	0000
83~82	BW Control Register for P03~P02	0x020B	0000
85~84	BW Control Register for P05~P04	0x020C	0000
87~86	BW Control Register for P07~P06	0x020D	0000
89~88	BW Control Register for P09~P08	0x020E	0000
8B~8A	BW Control Register for P11~P10	0x020F	0000
8D~8C	BW Control Register for P13~P12	0x0210	0000
8F~8E	BW Control Register for P15~P14	0x0211	0000
91~90	Reserved		
93~92	Reserved		
95~94	Reserved		

EEPROM Physical Address (8-Bit Data Entry) (24LC08)	Description	Corresponding Internal Register Address Mapping	Internal Default
97~96	BW Control Register for Gigabit and MII Port	0x0215	0000
99~98	Port VLAN ID Assignment0	0x030C	0100
9B~9A	Port VLAN ID Assignment1	0x030D	0302
9D~9C	Port VLAN ID Assignment2	0x030E	0504
9F~9E	Port VLAN ID Assignment3	0x030F	0706
A1~A0	Port VLAN ID Assignment4	0x0310	0908
A3~A2	Port VLAN ID Assignment5	0x0311	0B0A
A5~A4	Port VLAN ID Assignment6	0x0312	0D0C
A7~A6	Port VLAN ID Assignment7	0x0313	0F0E
A9~A8	Reserved		
AB~AA	Reserved		
AD~AC	Reserved		
AF~AE	Port VLAN ID Assignment8	0x0317	1716
B1~B0	Reserved		
B3~B2	VLAN TX Priority Tagging Control 0	0x0319	FFFF
B5~B4	VLAN TX Priority Tagging Control 1	0x031A	FFFF
B7~B6	VLAN TX Priority Tagging Control 2	0x031B	FFFF
B9~B8	Reserved		
BB~BA	Port VLAN Configuration0_0	0x031D	0001
BD~BC	Port VLAN Configuration0_1	0x031E	00C0
BF~BE	Port VLAN Configuration0_2	0x031F	0000
C1~C0	Port VLAN Configuration1_0	0x0320	0002
C3~C2	Port VLAN Configuration1_1	0x0321	00C0
C5~C4	Port VLAN Configuration1_2	0x0322	0000
C7~C6	Port VLAN Configuration2_0	0x0323	0004
C9~C8	Port VLAN Configuration2_1	0x0324	00C0
CB~CA	Port VLAN Configuration2_2	0x0325	0000
CD~CC	Port VLAN Configuration3_0	0x0326	0008
CF~CE	Port VLAN Configuration3_1	0x0327	00C0
D1~D0	Port VLAN Configuration3_2	0x0328	0000
D3~D2	Port VLAN Configuration4_0	0x0329	0010
D5~D4	Port VLAN Configuration4_1	0x032A	00C0
D7~D6	Port VLAN Configuration4_2	0x032B	0000
D9~D8	Port VLAN Configuration5_0	0x032C	0020
DB~DA	Port VLAN Configuration5_1	0x032D	00C0
DD~DC	Port VLAN Configuration5_2	0x032E	0000
DF~DE	Port VLAN Configuration6_0	0x032F	0040
E1~E0	Port VLAN Configuration6_1	0x0330	00C0
E3~E2	Port VLAN Configuration6_2	0x0331	0000
E5~E4	Port VLAN Configuration7_0	0x0332	0080
E7~E6	Port VLAN Configuration7_1	0x0333	00C0
E9~E8	Port VLAN Configuration7_2	0x0334	0000

EEPROM Physical Address (8-Bit Data Entry) (24LC08)	Description	Corresponding Internal Register Address Mapping	Internal Default
EB~EA	Port VLAN Configuration8_0	0x0335	0100
ED~EC	Port VLAN Configuration8_1	0x0336	00C0
EF~EE	Port VLAN Configuration8_2	0x0337	0000
F1~F0	Port VLAN Configuration9_0	0x0338	0200
F3~F2	Port VLAN Configuration9_1	0x0339	00C0
F5~F4	Port VLAN Configuration9_2	0x033A	0000
F7~F6	Port VLAN Configuration10_0	0x033B	0400
F9~F8	Port VLAN Configuration10_1	0x033C	00C0
FB~FA	Port VLAN Configuration10_2	0x033D	0000
FD~FC	Port VLAN Configuration11_0	0x033E	0800
FF~FE	Port VLAN Configuration11_1	0x033F	00C0
101~100	Port VLAN Configuration11_2	0x0340	0000
103~102	Port VLAN Configuration12_0	0x0341	1000
105~104	Port VLAN Configuration12_1	0x0342	00C0
107~106	Port VLAN Configuration12_2	0x0343	0000
109~108	Port VLAN Configuration13_0	0x0344	2000
10B~10A	Port VLAN Configuration13_1	0x0345	00C0
10D~10C	Port VLAN Configuration13_2	0x0346	0000
10F~10E	Port VLAN Configuration14_0	0x0347	4000
111~110	Port VLAN Configuration14_1	0x0348	00C0
113~112	Port VLAN Configuration14_2	0x0349	0000
115~114	Port VLAN Configuration15_0	0x034A	8000
117~116	Port VLAN Configuration15_1	0x034B	00C0
119~118	Port VLAN Configuration15_2	0x034C	0000
11B~11A	Port VLAN Configuration16_0	0x034D	0000
11D~11C	Port VLAN Configuration16_1	0x034E	00C1
11F~11E	Port VLAN Configuration16_2	0x034F	0000
121~120	Port VLAN Configuration17_0	0x0350	0000
123~122	Port VLAN Configuration17_1	0x0351	00C2
125~124	Port VLAN Configuration17_2	0x0352	0000
127~126	Port VLAN Configuration18_0	0x0353	0000
129~128	Port VLAN Configuration18_1	0x0354	00C4
12B~12A	Port VLAN Configuration18_2	0x0355	0000
12D~12C	Port VLAN Configuration19_0	0x0356	0000
12F~12E	Port VLAN Configuration19_1	0x0357	00C8
131~130	Port VLAN Configuration19_2	0x0358	0000
133~132	Port VLAN Configuration20_0	0x0359	0000
135~134	Port VLAN Configuration20_1	0x035A	00D0
137~136	Port VLAN Configuration20_2	0x035B	0000
139~138	Port VLAN Configuration21_0	0x035C	0000
13B~13A	Port VLAN Configuration21_1	0x035D	00E0
13D~13C	Port VLAN Configuration21_2	0x035E	0000
13F~13E	Port VLAN Configuration22_0	0x035F	FFFF

EEPROM Physical Address (8-Bit Data Entry) (24LC08)	Description	Corresponding Internal Register Address Mapping	Internal Default
141~140	Port VLAN Configuration22_1	0x0360	00FF
143~142	Port VLAN Configuration22_2	0x0361	0000
145~144	Port VLAN Configuration23_0	0x0362	FFFF
147~146	Port VLAN Configuration23_1	0x0363	00FF
149~148	Port VLAN Configuration23_2	0x0364	0000
14B~14A	Port VLAN Configuration24_0	0x0365	0000
14D~14C	Port VLAN Configuration24_1	0x0366	0000
14F~14E	Port VLAN Configuration24_2	0x0367	0000
151~150	Port VLAN Configuration25_0	0x0368	0000
153~152	Port VLAN Configuration25_1	0x0369	0000
155~154	Port VLAN Configuration25_2	0x036A	0000
157~156	Port VLAN Configuration26_0	0x036B	0000
159~158	Port VLAN Configuration26_1	0x036C	0000
15B~15A	Port VLAN Configuration26_2	0x036D	0000
15D~15C	Port VLAN Configuration27_0	0x036E	0000
15F~15E	Port VLAN Configuration27_1	0x036F	0000
161~160	Port VLAN Configuration27_2	0x0370	0000
163~162	Port VLAN Configuration28_0	0x0371	0000
165~164	Port VLAN Configuration28_1	0x0372	0000
167~166	Port VLAN Configuration28_2	0x0373	0000
169~168	Port VLAN Configuration29_0	0x0374	0000
16B~16A	Port VLAN Configuration29_1	0x0375	0000
16D~16C	Port VLAN Configuration29_2	0x0376	0000
16F~16E	Port VLAN Configuration30_0	0x0377	0000
171~170	Port VLAN Configuration30_1	0x0378	0000
173~172	Port VLAN Configuration30_2	0x0379	0000
175~174	Port VLAN Configuration31_0	0x037A	0000
177~176	Port VLAN Configuration31_1	0x037B	0000
179~178	Port VLAN Configuration31_2	0x037C	0000
17B~17A	Insert per-port VID enabling register0	0x037D	0000
17D~17C	Insert per-port VID enabling register1	0x037E	0000
17F~17E	Reserved		

Note: X=Not Configurable

10. Internal Register Descriptions

Symbols:

R:	Read	V:	Configurable
W:	Write	P:	Partially Configurable
RW:	Read/Write	X:	Not Configurable

10.1. System Configuration Register

Table 36. System Configuration Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0000	0	System Reset	RW	0	X	X
	1	Switch Parameter Register	R(W)	0x84A0	X	X
	2	EEPROM Check ID	R	0	X	V
	3	Reserved	R	0x0100	X	V
	4	LED MODE	RW	0001	X	X
	5	LED Display Configuration 0	RW	0E88	X	V
	6	LED Display Configuration 1	RW	0C00	X	V

10.2. System Status Register

Table 37. System Status Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0100	0	Board Trapping Status	R (/W)	0C01	X	X
	1	Loop Detect Status Register(32 bit Reg)	R	0	X	X
	2	System Fault Flag Register	R	0	X	X

10.3. Management Configuration Register

Table 38. Management Configuration Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0200	0	Realtek Protocol Control	RW	0001	X	V
	1	RRCP Security Mask Configuration (0)	RW	0	X	V
	2	RRCP Security Mask Configuration (1)	RW	0	X	V
	3	Switch MAC ID (0)	R	0	X	V
	4	Switch MAC ID (1)	R	0	X	V
	5	Switch MAC ID (2)	R	0	X	V
	6	Chip ID (RO)	R	0	X	V

Register Base Address	Offset	Description	RW	Default	Pin	EE
	7	Vender ID (0) (RO)	R	0	X	V
	8	Vender ID (1) (RO)	R	0	X	V
	9	RRCP Pass word	RW	0x2379	X	X
	0A	Port Rate Control Register.	RW	0	X	X
	0B	Port Rate Control Register.	RW	0	X	X
	0C	Port Rate Control Register.	RW	0	X	X
	0D	Port Rate Control Register.	RW	0	X	X
	0E	Port Rate Control Register.	RW	0	X	X
	0F	Port Rate Control Register.	RW	0	X	X
	10	Port Rate Control Register.	RW	0	X	X
	11	Port Rate Control Register.	RW	0	X	X
	12	Reserved	RW	0	X	X
	13	Reserved	RW	0	X	X
	14	Reserved	RW	0	X	X
	15	Gigabit port and MII port bandwidth control	RW	0	X	X
	16	Reserved		0		
	17	EEPROM RW Command Register	RW	0	X	X
	18	EEPROM RW Data Register	R(/W)	0	X	X
	19	Port Mirror Control Register for P15-P0	RW	0	X	X
	1A	Port Mirror Control Register for Gigabit , MII port	RW	0	X	X
	1B	RX Mirror port mask for P15-P0	RW	0	X	X
	1C	RX Mirror port mask for Gigabit , MII port	RW	0	X	X
	1D	TX Mirror port mask for P15-P0	RW	0	X	X
	1E	TX Mirror port mask for Gigabit , MII port	RW	0	X	X

10.4. Address Lookup Table (ALT) Control Register

Table 39. Address Lookup Table (ALT) Control Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0300	0	ALT Configuration	RW	0	P	P
	1	Address Learning Control (0)	RW	0	X	X
	2	Address Learning Control (1)	RW	0	X	X
	3	Unknown SA Management 0 (RO) (0)	R	--	X	X
	4	Unknown SA Management 0 (RO) (1)	R	--	X	X
	5	Unknown SA Management 0 (RO) (2)	R	--	X	X
	6	Unknown SA Management 1(RO)	R	--	X	X
	7	Port Trunking Configuration	RW	8200	P	V
	8	IGMP Control Register	RW	8200	V	V
	9	IP Multicast Router Discovery	R	0	X	X
	0A	Reserved				
	0B	VLAN Control Register	RW	0	P	V
	0C	Port VLAN ID Assignment (0) [P1P0]	RW	0100	X	X

Register Base Address	Offset	Description	RW	Default	Pin	EE
	0D	Port VLAN ID Assignment (1) [P3P2]	RW	0302	X	X
	0E	Port VLAN ID Assignment (2) [P5P4]	RW	0504	X	X
	0F	Port VLAN ID Assignment (3) [P7P6]	RW	0706	X	X
	10	Port VLAN ID Assignment (4) [P9P8]	RW	0908	X	X
	11	Port VLAN ID Assignment (5) [P11P10]	RW	0B0A	X	X
	12	Port VLAN ID Assignment (6) [P13P12]	RW	0D0C	X	X
	13	Port VLAN ID Assignment (7) [P15P14]	RW	0F0E	X	X
	14	Port VLAN ID Assignment (8) (Reserved)	RW	1110	X	X
	15	Port VLAN ID Assignment (9) (Reserved)	RW	1312	X	X
	16	Port VLAN ID Assignment (10) (Reserved	RW	1514	X	X
	17	Port VLAN ID Assignment (11) [M0,G0]	RW	1716	X	X
	18	Reserved				
	19	VLAN TX Priority Tagging Control (0)	RW	FFFF	X	X
	1A	VLAN TX Priority Tagging Control (1)	RW	FFFF	X	X
	1B	VLAN TX Priority Tagging Control (2)	RW	FFFF	X	X
	1C	Reserved				
		Port VLAN Configuration (32*[0,1,2])	RW		X	X
	1D	VLAN_0_Entry_Configuration_0 (member[15:0])	RW	0001	X	X
	1E	VLAN_0_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00C0	X	X
	1F	VLAN_0_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	20	VLAN_1_Entry_Configuration_0 (member[15:0])	RW	0002	X	X
	21	VLAN_1_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00C0	X	X
	22	VLAN_1_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	23	VLAN_2_Entry_Configuration_0 (member[15:0])	RW	0004	X	X
	24	VLAN_2_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00C0	X	X
	25	VLAN_2_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	26	VLAN_3_Entry_Configuration_0 (member[15:0])	RW	0008	X	X
	27	VLAN_3_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00C0	X	X
	28	VLAN_3_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	29	VLAN_4_Entry_Configuration_0 (member[15:0])	RW	0010	X	X
	2A	VLAN_4_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00C0	X	X
	2B	VLAN_4_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	2C	VLAN_5_Entry_Configuration_0 (member[15:0])	RW	0020	X	X
	2D	VLAN_5_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00C0	X	X
	2E	VLAN_5_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	2F	VLAN_6_Entry_Configuration_0 (member[15:0])	RW	0040	X	X
	30	VLAN_6_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00C0	X	X
	31	VLAN_6_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	32	VLAN_7_Entry_Configuration_0 (member[15:0])	RW	0080	X	X

Register Base Address	Offset	Description	RW	Default	Pin	EE
	33	VLAN_7_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00C0	X	X
	34	VLAN_7_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	35	VLAN_8_Entry_Configuration_0 (member[15:0])	RW	0100	X	X
	36	VLAN_8_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	01C0	X	X
	37	VLAN_8_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	38	VLAN_9_Entry_Configuration_0 (member[15:0])	RW	0200	X	X
	39	VLAN_9_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	02C0	X	X
	3A	VLAN_9_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	3B	VLAN_10_Entry_Configuration_0 (member[15:0])	RW	0400	X	X
	3C	VLAN_10_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	04C0	X	X
	3D	VLAN_10_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	3E	VLAN_11_Entry_Configuration_0 (member[15:0])	RW	0800	X	X
	3F	VLAN_11_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	08C0	X	X
	40	VLAN_11_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	41	VLAN_12_Entry_Configuration_0 (member[15:0])	RW	1000	X	X
	42	VLAN_12_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	10C0	X	X
	43	VLAN_12_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	44	VLAN_13_Entry_Configuration_0 (member[15:0])	RW	2000	X	X
	45	VLAN_13_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	20C0	X	X
	46	VLAN_13_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	47	VLAN_14_Entry_Configuration_0 (member[15:0])	RW	4000	X	X
	48	VLAN_14_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	40C0	X	X
	49	VLAN_14_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	4A	VLAN_15_Entry_Configuration_0 (member[15:0])	RW	8000	X	X
	4B	VLAN_15_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	80C0	X	X
	4C	VLAN_15_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	4D	VLAN_16_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	4E	VLAN_16_Entry_Configuration_1 (member[23: 22]) *NOTE(1)*	RW	00C1	X	X
	4F	VLAN_16_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	50	VLAN_17_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	51	VLAN_17_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00C2	X	X
	52	VLAN_17_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	53	VLAN_18_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	54	VLAN_18_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00C4	X	X
	55	VLAN_18_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	56	VLAN_19_Entry_Configuration_0 (member[15:0])	RW	0000	X	X

Register Base Address	Offset	Description	RW	Default	Pin	EE
	57	VLAN_19_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00C8	X	X
	58	VLAN_19_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	59	VLAN_20_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	5A	VLAN_20_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00D0	X	X
	5B	VLAN_20_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	5C	VLAN_21_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	5D	VLAN_21_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	00E0	X	X
	5E	VLAN_21_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	5F	VLAN_22_Entry_Configuration_0 (member[15:0])	RW	FFFF	X	X
	60	VLAN_22_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	FFFF	X	X
	61	VLAN_22_Entry_Configuration_2 (VID[11:0])	RW	F000	X	X
	62	VLAN_23_Entry_Configuration_0 (member[15:0])	RW	FFFF	X	X
	63	VLAN_23_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	FFFF	X	X
	64	VLAN_23_Entry_Configuration_2 (VID[11:0])	RW	F000	X	X
	65	VLAN_24_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	66	VLAN_24_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	0000	X	X
	67	VLAN_24_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	68	VLAN_25_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	69	VLAN_25_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	0000	X	X
	6A	VLAN_25_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	6B	VLAN_26_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	6C	VLAN_26_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	0000	X	X
	6D	VLAN_26_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	6E	VLAN_27_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	6F	VLAN_27_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	0000	X	X
	70	VLAN_27_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	71	VLAN_28_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	72	VLAN_28_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	0000	X	X
	73	VLAN_28_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	74	VLAN_29_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	75	VLAN_29_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	0000	X	X
	76	VLAN_29_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	77	VLAN_30_Entry_Configuration_0 (member[15:0])	RW	0000	X	X
	78	VLAN_30_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	0000	X	X
	79	VLAN_30_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	7A	VLAN_31_Entry_Configuration_0 (member[15:0])	RW	0000	X	X

Register Base Address	Offset	Description	RW	Default	Pin	EE
	7B	VLAN_31_Entry_Configuration_1 (member[23:22]) *NOTE(1)*	RW	0000	X	X
	7C	VLAN_31_Entry_Configuration_2 (VID[11:0])	RW	0000	X	X
	7D	Insert per-port VID enabling register	RW	0	X	V
	7E	Insert per-port VID enabling register	RW	0	X	V

Note 1: Member[23:22] mapping to MII port and Gigabit Port

10.5. Queue Control Register

Table 40. Queue Control Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0400	0	QoS Control Register	RW	0	V	V
	1	Port Priority Configuration (0)	RW	0	V	V
	2	Port Priority Configuration (1)	RW	0	V	V
	8	Reserved (Used by RRCP software)	RW	0	V	V

10.6. PHY Access Control Register

Table 41. PHY Access Control Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0500	0	PHY Access Addressing Control	R(/W)	0	X	X
	1	PHY Access Write Data	RW	--	X	X
	2	PHY Access Read Data	R	--	X	X

10.7. Port Control Register

Table 42. Port Control Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0600	0~6	Reserved				
	7	Global Port Control Register	RW	0010	V	V
	8	Port Access Authority Control (0)	RW	0	X	X
	9	Port Access Authority Control (1)	RW	0	X	X
	A	Port Property Configuration Register 0 (Port 0, 1)	RW	AFAF	X	V
	B	Port Property Configuration Register 1 (Port 2, 3)	RW	AFAF	X	V
	C	Port Property Configuration Register 2 (Port 4, 5)	RW	AFAF	X	V
	D	Port Property Configuration Register 3 (Port 6, 7)	RW	AFAF	X	V
	E	Port Property Configuration Register 4 (Port 8, 9)	RW	AFAF	X	V
	F	Port Property Configuration Register 5 (Port 10, 11)	RW	AFAF	X	V
	10	Port Property Configuration Register 6 (Port 12, 13)	RW	AFAF	X	V
	11	Port Property Configuration Register 7 (Port 14, 15)	RW	AFAF	X	V
	12	Port Property Configuration Register 8 (Reserved)	RW	AFAF	X	V
	13	Port Property Configuration Register 9 (Reserved)	RW	AFAF	X	V
	14	Port Property Configuration Register 10 (Reserved)	RW	AFAF	X	V
	15	Port Property Configuration Register 11 (Gigabit, MII) Port	RW	AFAF	X	V
	16	Reserved				
	17	Reserved				
	18	Reserved[15:2], SyncOk [1:0]	R		X	X
	19	Port Link Status Register 0 (Port 0, 1)	R	0	X	X
	1A	Port Link Status Register 1 (Port 2, 3)	R	0	X	X
	1B	Port Link Status Register 2 (Port 4, 5)	R	0	X	X
	1C	Port Link Status Register 3 (Port 6, 7)	R	0	X	X
	1D	Port Link Status Register 4 (Port 8, 9)	R	0	X	X
	1E	Port Link Status Register 5 (Port 10, 11)	R	0	X	X
	1F	Port Link Status Register 6 (Port 12, 13)	R	0	X	X
	20	Port Link Status Register 7 (Port 14, 15)	R	0	X	X
	21	Port Link Status Register 8 (Reserved)	R	0	X	X
	22	Port Link Status Register 9 (Reserved)	R	0	X	X
	23	Port Link Status Register 10 (Reserved)	R	0	X	X
	24	Port Link Status Register 11 (Gigabit, MII) Port	R	0	X	X
	25	Reserved				
	26	Reserved				
	27	Reserved				
	28	Reserved				

10.8. MIB Counter Register

Table 43. MIB Counter Register

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0700	0	Port MIB Counter Object Selection Register 0 (Port 0, 1)	RW	0555	X	X
	1	Port MIB Counter Object Selection Register 1 (Port 2, 3)	RW	0555	X	X
	2	Port MIB Counter Object Selection Register 2 (Port 4, 5)	RW	0555	X	X
	3	Port MIB Counter Object Selection Register 3 (Port 6, 7)	RW	0555	X	X
	4	Port MIB Counter Object Selection Register 4 (Port 8, 9)	RW	0555	X	X
	5	Port MIB Counter Object Selection Register 5 (Port 10, 11)	RW	0555	X	X
	6	Port MIB Counter Object Selection Register 6 (Port 12, 13)	RW	0555	X	X
	7	Port MIB Counter Object Selection Register 7 (Port 14, 15)	RW	0555	X	X
	8	Port MIB Counter Object Selection Register 8 (Reserved)	RW	0555	X	X
	9	Port MIB Counter Object Selection Register 9 (Reserved)	RW	0555	X	X
	A	Port MIB Counter Object Selection Register 10 (Reserved)	RW	0555	X	X
	B	Port MIB Counter Object Selection Register 11 (Gigabit, MII) Port	RW	0555	X	X
	C	Reserved				

10.8.1. Port MIB Counter 1 Register (RX Counter) (32-bits)

Table 44. Port MIB Counter 1 Register (RX Counter) (32-bits)

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0700	D	Port 0 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	E	Port 1 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	F	Port 2 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	10	Port 3 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	11	Port 4 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	12	Port 5 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	13	Port 6 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	14	Port 7 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	15	Port 8 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	16	Port 9 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	17	Port 10 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	18	Port 11 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	19	Port 12 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	1A	Port 13 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	1B	Port 14 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	1C	Port 15 MIB Counter 1 Register (RX Counter) (32-bits)	R	0	X	X
	1D	Reserved	R	0	X	X
	1E	Reserved	R	0	X	X
	1F	Reserved	R	0	X	X
	20	Reserved	R	0	X	X
	21	Reserved	R	0	X	X

Register Base Address	Offset	Description	RW	Default	Pin	EE
	22	Reserved	R	0	X	X
	23	(Gigabit Port) Counter 1 Register (RX Counter) (32-bit)	R	0	X	X
	24	(MII Port) MIB Counter 1 Register (RX Counter) (32-bit)	R	0	X	X
	25	Reserved				
	26	Reserved				

10.8.2. Port MIB Counter 2 Register (TX Counter) (32-bits)

Table 45. Port MIB Counter 2 Register (TX Counter) (32-bits)

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0700	27	Port 0 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	28	Port 1 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	29	Port 2 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2A	Port 3 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2B	Port 4 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2C	Port 5 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2D	Port 6 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2E	Port 7 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	2F	Port 8 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	30	Port 9 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	31	Port 10 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	32	Port 11 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	33	Port 12 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	34	Port 13 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	35	Port 14 MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	36	Reserved Port 15MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	37	Reserved				
	38	Reserved				
	39	Reserved				
	3A	Reserved				
	3B	Reserved				
	3C	Reserved				
	3D	(Gigabit Port) MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	3E	(MII Port) MIB Counter 2 Register (TX Counter) (32-bits)	R	0	X	X
	3F	Reserved				
	40	Reserved				

10.8.3. Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)

Table 46. Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)

Register Base Address	Offset	Description	RW	Default	Pin	EE
0x0700	41	Port 0 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	42	Port 1 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	43	Port 2 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	44	Port 3 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	45	Port 4 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	46	Port 5 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	47	Port 6 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	48	Port 7 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	49	Port 8 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4A	Port 9 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4B	Port 10 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4C	Port 11 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4D	Port 12 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4E	Port 13 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	4F	Port 14 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	50	Port 15 MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	51	Reserved				
	52	Reserved				
	53	Reserved				
	54	Reserved				
	55	Reserved				
	56	Reserved				
	57	(Gigabit Port) MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	58	(MII Port) MIB Counter 3 Register (Diagnostic Counter)(32-bits)	R	0	X	X
	59	Reserved				
	5A	Reserved				

10.9. System Parameter Register (Reserved)

Table 47. System Parameter Register (Reserved)

Register Base Address	Offset	Description	RW	Default	Pin	EE
0xFFFF	--	System Parameter Register (Reserved).	RW	0	V	V

11. Internal Register Settings

Register Symbols:

R:	Read	LL:	Latch Low until cleared
W:	Write	LH:	Latch High until cleared
RW:	Read/Write	SC:	Self Clearing
(W: EEPROM. Permit writing by EEPROM)		RC:	Read to Clear

11.1. System Configuration Register

11.1.1. 0x0000H: System Reset Control Register

Table 48. 0x0000H: System Reset Control Register

Bits	Name	Description	RW	Default
0	SRST	Soft Reset. A soft reset will reset the system similar to a power on reset except that the user configuration will not be cleared: 1. The MAC table and VLAN table data are kept. 2. All current user configured internal register values are kept. 3. The EEPROM download is not done again. 4. The system restarts the auto-negotiation process. 0: Normal (Default) 1: Soft reset	W/SC	0
1	HRST	Hardware Reset. Resets the system to the power on initial state: 1. Downloads configuration from strap pin and EEPROM. 2. Starts internal Memory self test. 3. Clears all the MAC, VLAN tables. 4. Resets all registers to default values. 5. Restarts auto-negotiation. 0: Normal (Default) 1: Hardware reset	W/SC	0
15:2	Reserved			

11.1.2. 0x0001H: Switch Parameter Register

Note: The Write operation is reserved for IC testing mode. Do NOT write this register.

Table 49. 0x0001H: Switch Parameter Register

Bits	Name	Description	RW	Default
1:0	MaxPktLen[1:0]	System Valid Max Packet Length. The minimum packet length is 64 bytes. The maximum packet length is controlled by MaxPktLen[1:0]: 00: 1536 bytes (Default) 01: 1552 byte 1x: Reserved.	RW	00 HW pin MaxPktLen
2	TXIPG_Comp	Transmit IPG Compensation. Used to compensate the oscillator frequency or incoming packet Inter-Packet Gap (IPG) tolerance. 0: Give +65 ppm TXIPG compensation (Default) 1: Give +90 ppm TXIPG compensation	RW	0
3	MaxPauseCnt	Max Pause Count for Congestion Control. 0: Supports a maximum of 128 Pause frames during congestion control (Default) 1: Continue Pause mode. Do not limit the Pause frame count during congestion control.	RW	0 HW pin MaxPauseCnt
4	DisBKP48One ($\overline{\text{EnBKP48One}}$)	Disable Back pressure 48 Pass One Algorithm. When the 48One algorithm is enabled, the switch will pass one incoming packet after every 48 collisions. 0: Enable 48 Pass One algorithm (Default) 1: Disable 48 Pass One algorithm	RW	0 HW pin EnBKP48One
6:5	Reserved	Internal test bit.		
7	DisCRSBKPMode ($\overline{\text{EnCOLBKPMode}}$)	Disable Carrier Based Back Pressure Mode. Half duplex back pressure algorithm selection. 0: Select Collision-based back pressure mode 1: Select Carrier-based back pressure mode (Default)	RW	1 HW pin EnCOLBKPmode
15:8	Reserved	Internal test bit.		

11.1.3. 0x0002H: EEPROM Check ID

Table 50. 0x0002H: EEPROM Check ID

Bits	Name	Description	RW	Default
5:0	Reserved (EEPROM Check ID)	Reserved bits. Used for EEPROM existence checking. Keep the value at 000000.		
15:6	Reserved	Internal test bit.		

11.1.4. 0x0004H: General Purpose User Defined I/O Data Register

Table 51. 0x0004H: General Purpose User Defined I/O Data Register

Bits	Name	Description	RW	Default
1:0	LED MODE	00: Scan Led 01: Single-color serial (default) 10: Bi-color serial 11: Reserved	RW	01 HW pin P9TXD P8TXD
15:2	Reserved			

11.1.5. 0x0005H: LED Display Configuration

Table 52. 0x0005H: LED Display Configuration

Bits	Name	Description	RW	Default
2:0	StatLED0_mode[2:0]	Mode Selection for State LED0. This state LED mode selection register controls the status type of the State LED0. The Status type is defined as follows: 000: Link/Act (Default) 001: 100Spd 010: Duplex/Col 011: Link/Act/100Spd 100: Duplex 101: Act 110: Link 111: Col	RW	000
5:3	StatLED1_mode[2:0]	Mode Selection for State LED1. 000: Link/Act 001: 100Spd (Default) 010: Duplex/Col 011: Link/Act/100Spd 100: Duplex 101: Act 110: Link 111: Col	RW	001
8:6	StatLED2_mode[2:0]	Mode Selection for State LED2. 000: Link/Act 001: 100Spd 010: Duplex/Col (Default) 011: Link/Act/100Spd 100: Duplex 101: Act 110: Link 111: Col	RW	010

Bits	Name	Description	RW	Default
12:9	EnLED[3:0]	State LED 0, 1, 2 and Diagnostic LED Enable/Disable Control. EnLED[3:0] controls enabling/disabling of DiagLED, StatLED2, StatLED1, StatLED0. 0: Disable 1: Enable If an LED is disabled, the corresponding serial clock will be masked.	RW	0111
14:13	Diagnostic mode		RW	00
15	Reserved			

11.2. System Status Register

11.2.1. 0x0100H: Board Trapping Status Register

Table 53. 0x0100H: Board Trapping Status Register

Bits	Name	Description	RW	Default
0	EEPROM_detect_ status	EEPROM Existence Status. 0: Exists (Default) 1: Does not Exist	R	0
15:2	Reserved			

11.2.2. 0x0101H: Loop Detect Status Register (32-Bit Register)

Table 54. 0x0101H: Loop Detect Status Register (32-Bit Register)

Bits	Name	Description	RW	Default
23:0	LoopDetPort[23:0]	Network Loop event Detect Port Status. If the loop detect function is enabled, the corresponding bit of LoopDetPort[23:0] will be set whenever a loop event is detected on the corresponding switch port. The set bit is cleared only when the loop event has disappeared on that port. When the loop detect function is enabled, the switch will periodically transmit one loop detect diagnostic frame. The normal interval time is approx. five minutes. When a loop event is detected, the interval time will be changed to fast mode. In fast mode the interval time is about 1 second in order to accelerate detection and diagnostic. The loop event will be reported in this Loop Detect Status Register. 0: No Loop detected on this port (Default) 1: Loop detected on this port [15:0] mapping to P15~P0 [22] mapping to Gigabit port [23] mapping to MII port	R	0
31:24	Reserved			

11.2.3. 0x0102H: System Fault Indication Register

Table 55. 0x0102H: System Fault Indication Register

Bits	Name	Description	RW	Default
0	Reserved			
1	TrunkFault	Trunk Fault event flag. The flag indicates that there is a trunk port member link down. The trunk will still continue to operate due to the trunk auto fault recovery algorithm. 0: No trunk fault detected (Default) 1: Trunk fault detected	R	0
2	LoopFault	Network Loop Fault Indication. When the Loop Fault indication is set, a loop detected port will be reported on the Loop Detect Port Register. 0: Network Loop not detected (Default) 1: Network Loop detected	R	0
5:3	Reserved			
9:6	FaultTkGroup[3:0]	The Fault Trunk Group Indicator. Indicates a Link Fault in the trunk group. A physical link failure of an enabled trunk group will cause the corresponding bit to be set in the FaultTkGroup[5:0]. This is a real time fault status report. Even though the Trunk Group's fault occurred and the fault bit is set, the corresponding trunk can still work properly as fault recovery will be auto applied. FaultTkGroup[0] indicator for Trunk 1: (port 0, 1, 2, 3) FaultTkGroup[1] indicator for Trunk 2: (port 4, 5, 6, 7) FaultTkGroup[2] indicator for Trunk 3: (port 8, 9, 10, 11) FaultTkGroup[3] indicator for Trunk 4: (port 12, 13, 14, 15) 0: Trunk OK 1: Trunk Fault detected	R	000000
15:12	Reserved			

11.3. Management Configuration Register

11.3.1. 0x0200H: Realtek Protocol Control Register

Table 56. 0x0200H: Realtek Protocol Control Register

Bits	Name	Description	RW	Default
0	DisRRCP (EnRRCP)	Disable Realtek Remote Control Protocol (RRCP). 0: Enable RRCP 1: Disable RRCP (Default)	RW	1 HW pin: EnRRCP
1	DisREcho	Disable Realtek Remote Echo Protocol. 0: Enable REcho protocol. (Default) 1: Disable REcho protocol.	RW	0
2	EnLoopDet	Enable Loop Detect Function. When enabled, the loop detect status will be reported in register 0x0101 (Loop Detect Status Register). 0: Disable(Default) 1: Enable	RW	0
15:3	Reserved			

11.3.2. 0x0201H: RRCP Security Mask Configuration Register 0

Table 57. 0x0201H: RRCP Security Mask Configuration Register 0

Bits	Name	Description	RW	Default
15:0	RRCP_SMask[15:0]	RRCP Management Security Mask Configuration. Configuration for ports 0 to 15. Specifies which port's incoming RRCP access commands will be responded to. 0: RRCP Access enabled port (Default) 1: RRCP Access disabled port *Note: Ports 0~15, Gigabit and MII ports' RRCP security mask will be set if the hardware strap pin EnHomeVlan is pulled high during power on reset. This can be overwritten by EEPROM or registers access.*	RW	0

11.3.3. 0x0202H: RRCP Security Mask Configuration Register 1

Table 58. 0x0202H: RRCP Security Mask Configuration Register 1

Bits	Name	Description	RW	Default
7:6	RRCP_SMask[23:22]	RRCP Management Security Mask Configuration. RRCP_SMask [22] is configuration for gigabit port RRCP_SMask [23] is configuration for MII port. Specifies which port's incoming RRCP access commands will be responded to. 0: RRCP Access enabled port (Default) 1: RRCP Access disabled port *Note: Ports 0~15, Gigabit and MII ports' RRCP security mask will be set if the hardware strap pin EnHomeVlan is pulled high during power on reset. This can be over written by EEPROM or registers access.*	RW	0

11.3.4. 0x0203H: Switch MAC ID Register 0

Table 59. 0x0203H: Switch MAC ID Register 0

Bits	Name	Description	RW	Default
15:0	MACID[15:0]	Switch Physical MAC Address bit[15:0]. E.g., For the 48-bit MAC address '52-54-4C-01-02-03', then MACID[15:0]=54-52.	R (W: EEPROM)	0

11.3.5. 0x0204H: Switch MAC ID Register 1

Table 60. 0x0204H: Switch MAC ID Register 1

Bits	Name	Description	RW	Default
15:0	MACID[31:16]	Switch Physical MAC Address bit[31:16] E.g., For the 48-bit MAC address '52-54-4C-01-02-03', then MACID[15:0]=54-52.	R (W: EEPROM)	0

11.3.6. 0x0205H: Switch MAC ID Register 2

Table 61. 0x0205H: Switch MAC ID Register 2

Bits	Name	Description	RW	Default
15:0	MACID[47:32]	Switch Physical MAC Address bit[47:32]. E.g., For the 48-bit MAC address '52-54-4C-01-02-03', then MACID[15:0]=54-52.	R (W: EEPROM)	0

11.3.7. 0x0206H: Chip Model ID

Table 62. 0x0206H: Chip Model ID

Bits	Name	Description	RW	Default
7:0	ChipID[7:0]	Chip ID. Identifies the chip version for programmer version control.	R (W: EEPROM)	0
15:8	Reserved			

11.4. 0x0207H: System Vender ID Register 0

Table 63. 0x0207H: System Vender ID Register 0

Bits	Name	Description	RW	Default
15:0	VenderID[15:0]	System Vender Identity Stream [15:0]. Used for the system vender to fill a code or name stream for switch device model number or vender name identification.	R (W: EEPROM)	0

11.5. 0x0208H: System Vender ID Register 1

Table 64. 0x0208H: System Vender ID Register 1

Bits	Name	Description	RW	Default
15:0	VenderID[31:16]	System Vender Identity Stream [31:16]. Used for system vender to fill a code or name stream for switch device model number or vender name identification.	R (W: EEPROM)	0

11.6. 0x0209H: RRCP Authentication Key Configuration Register

Table 65. 0x0209H: RRCP Authentication Key Configuration Register

Bits	Name	Description	RW	Default
15:0	RRCP_KEY[15:0]	RRCP Access Authentication Key Configuration. After power on reset, the RRCP Authentication Key is set to the default value '0x2379'. It can be updated via the CPU interface or by an RRCP control frame with a correct current authentication key value in the frame. The Authentication Key checking rule for RRCP frames is defined as follows: 1. For the Hello command frame: -- Broadcast Hello frame: Do not check Auth. Key. -- Unicast Hello frame: Auth. Key = RRCP_KEY[15:0] *Note 1: When the RRCP_KEY[15:0] is updated by the user, only unicast Hello frames are valid.* *Note 2: For a Get/Set command frame: Always uses the current key value defined by RRCP_KEY[15:0]*	RW	0x2379

11.7. 0x020AH: Port 0, 1 Bandwidth Control Register

Table 66. 0x020AH: Port 0, 1 Bandwidth Control Register

Bits	Name	Description	RW	Default
3:0	P0RXRate[3:0]	Port 0 RX Bandwidth Control. Configures the maximum output bandwidth of the port. Bit 3 is a reserved bit. Bit[2:0] controls the maximum RX rate of the port. 000: Disables rate control (Default) 001: 128Kbps 010: 256Kbps 011: 512Kbps 100: 1Mbps 101: 2Mbps 110: 4Mbps 111: 8Mbps	RW	0000

Bits	Name	Description	RW	Default
7:4	P0TXRate[3:0]	Port 0 TX Bandwidth Control. Configures the maximum input bandwidth of the port. Bit 3 is a reserved bit. Bit[2:0] controls the maximum TX rate of the port. 000: Disables rate control (Default) 001: 128Kbps 010: 256Kbps 011: 512Kbps 100: 1Mbps 101: 2Mbps 110: 4Mbps 111: 8Mbps	RW	0000
11:8	P1RXRate[3:0]	Port 1 RX Bandwidth Control. Configures the maximum output bandwidth of the port. Bit 3 is a reserved bit. Bit[2:0] controls the maximum RX rate of the port. 000: Disables rate control (Default) 001: 128Kbps 010: 256Kbps 011: 512Kbps 100: 1Mbps 101: 2Mbps 110: 4Mbps 111: 8Mbps	RW	0000
15:12	P1TXRate[3:0]	Port 1 TX Bandwidth Control. Configures the maximum input bandwidth of the port. Bit 3 is a reserved bit. Bit[2:0] controls the maximum TX rate of the port. 000: Disables rate control (Default) 001: 128Kbps 010: 256Kbps 011: 512Kbps 100: 1Mbps 101: 2Mbps 110: 4Mbps 111: 8Mbps	RW	0000

11.8. 0x020BH~0x0211H , 0x0215: Port 2~15, Gigabit Port and MII Port Bandwidth Control Register

Refer to Table 66, page 73, for Configuration description of n: 1 ~ 7, and n=11.

Table 67. 0x020BH~0x0211H: Port 2~15 Gigabit port and MII port Bandwidth Control Register

Bits	Name	Description	RW	Default
3:0	P2nRXRate[3:0]	Port 2n RX Bandwidth Control	RW	0000
7:4	P2nTXRate[3:0]	Port 2n TX Bandwidth Control	RW	0000
11:8	P2n+1RXRate[3:0]	Port 2n+1 RX Bandwidth Control	RW	0000
15:12	P2n+1TXRate[3:0]	Port 2n+1 TX Bandwidth Control	RW	0000

11.9. 0x0217H~0x0218: EEPROM RW Control Register

11.9.1. 0x0217H: EEPROM RW Command Register

Table 68. 0x0217H: EEPROM RW Command Register

Bits	Name	Description	RW	Default
7:0	EEPROM address	Assigns EEPROM address bits	RW	0
10:8	CHIP_SEL[2:0]]	Assigns chip selection bits	RW	0
11	Read/Write Operation	0: Write Operation 1: Read Operation	RW	0
12	Status	0: Idle 1: Busy	RW	0
13	Operation Succeeded status	0: Operation Succeeded 1: Operation Fail (Read Clear)	RW	0
15:14	Reserved			

11.9.2. 0x0218H: EEPROM RW Data Register

Table 69. 0x0218H: EEPROM RW Data Register

Bits	Name	Description	RW	Default
7:0	WdataEE[7:0]	Data to be written to EEPROM	RW	0
15:8	RdataEE[15:8]	Data Read from EEPROM	R	0

11.10. 0x0219H~0x021EH: Port Mirror Control Register

11.10.1. 0x0219H: Port Mirror Control Register 0 for P15-P0

Table 70. Port Mirror Control Register for P15-P0

Bits	Name	Description	RW	Default
15:0	EnPortMirror(0)[15:0]	Enables the port-based mirror function. Bit n corresponds to port n. Write '1' to enable a port's mirror function.	RW	0

11.10.2. 0x021AH: Port Mirror Control Register 1 for Gigabit and MII Ports

Table 71. Port Mirror Control Register for Gigabit and MII ports

Bits	Name	Description	RW	Default
5:0	Reserved			
7:6	EnPortMirror(1)[6:0]	Enables the port-based mirror function. Write '1' to enable a port's mirror function Bit [6]: Gigabit Port control bit Bit [7]: MII Port control bit	RW	0
15:8	Reserved			

11.10.3. 0x021BH: RX Mirror Port Register 0 for P15-P0

Table 72. RX Mirror Port Register 0 for P15-P0

Bits	Name	Description	RW	Default
15:0	Mirror_RX(0)[15:0]	Bit n corresponds to port n. Write '1' to duplicate port n RX data to mirrored port.	RW	0

11.10.4. 0x021CH: RX Mirror Port Register 1 for Gigabit and MII Ports

Table 73. RX Mirror Port Register 1 for Gigabit and MII ports

Bits	Name	Description	RW	Default
5:0	Reserved			
7:6	Mirror_RX(1)[7:6]	Bit [6]: Gigabit Port control bit Bit [7]: MII Port control bit Write '1' to duplicate port n RX data to mirrored port.	RW	0
15:8	Reserved			

11.10.5. 0x021DH: TX Mirror Port Register 0 for P15-P0

Table 74. TX Mirror Port Register 0 for P15-P0

Bits	Name	Description	RW	Default
15:0	Mirror_TX(0)[15:0]	Bit n corresponds to port n. Write '1' to duplicate port n TX data to mirrored port	RW	0

11.10.6. 0x021EH: TX Mirror Port Register 1 for Gigabit and MII Ports

Table 75. RX Mirror Port Register 1 for Gigabit and MII ports

Bits	Name	Description	RW	Default
5:0	Reserved			
7:6	Mirror_TX(1)[7:6]	Bit [6]: Gigabit Port control bit Bit [7]: MII Port control bit Write '1' to duplicate port n TX data to mirrored port	RW	0
15:8	Reserved			

11.11. Address Lookup Table (ALT) Control Register

11.11.1. 0x0300H: ALT Configuration Register

Table 76. 0x0300H: ALT Configuration Register

Bits	Name	Description	RW	Default
0	DisMacAging	Global Disable Mac Table Aging Function. 0: Enable Aging function (Default) 1: Disable Aging function	RW	0
1	EnFastAgeTime	Enable Fast Aging Time Mode. 0: Disable Fast Aging time; Aging set to 300 seconds (Default) 1: Enable Fast Aging time; Aging set to 12 seconds	RW	0
2	EnCtrlFFilter	Global Enable 802.1D Specified Reserved Control Frame Filtering. When network control packets are received with a destination MAC address as the group MAC address: (01-80-C2-00-00-04 ~ 01-80-C2-00-00-0F), the switch will drop the packets if the bit EnCtrlFilter=1. Otherwise (EnCtrlFilter=0) they will be flooded. 1: Enable Filtering (Default) 0: Disable Filtering	RW	1 HW pin. EnCtrlFFilter
3	EnDropUknDA	Internal test bit.	RW	0
15:4	Reserved			

11.11.2. 0x0301H: Address Learning Control Register 0

Table 77. 0x0301H: Address Learning Control Register 0

Bits	Name	Description	RW	Default
15:0	DisMacLearn[15:0]	Per-Port Disable Mac Address Learning Function (Ports 0~15). DisMacLearn[15:0] control port[15:0]. The Layer 2 MAC address learning function can be per-port disabled for security management purposes. Generally this register is used with the ALT Configuration Register (0x0300) bits 'DisMacAging'. 0: Enable learning (Default) 1: Disable learning	RW	0

11.11.3. 0x0302H: Address Learning Control Register 1

Table 78. 0x0302H: Address Learning Control Register 1

Bits	Name	Description	RW	Default
7:6	DisMacLearn[23:22]	Per-Port Disable Mac Address Learning Function DisMacLearn[23:22] control gigabit and MII ports Bit [22]: Gigabit Port control bit Bit [23]: MII Port control bit The Layer 2 MAC address learning function can be per-port disabled for security management purposes. Generally this register is used with the ALT Configuration Register (0x0300H) bits 'DisMacAging' &. 0: Enable learning (Default) 1: Disable learning	RW	0
15:8	Reserved			

11.11.4. 0x0307H: Port Trunking Configuration Register

Table 79. 0x0307H: Port Trunking Configuration Register

Bits	Name	Description	RW	Default
0	Reserved			
4:1	EnTrunk[3:0]	Trunk Group Enable/Disable Control. Enables trunk groups. EnTrunk[0] control for Trunk 1: (port 0, 1, 2, 3). EnTrunk[1] control for Trunk 2: (port 4, 5, 6, 7). EnTrunk[2] control for Trunk 3: (port 8, 9, 10, 11). EnTrunk[3] control for Trunk 4: (port 12, 13, 14, 15). 0: Disable Trunking (Default) 1: Enable Trunking	RW	0x00
15:7	Reserved			

11.11.5. 0x0308H: IGMP Snooping Control Register

Table 80. 0x0308H: IGMP Snooping Control Register

Bits	Name	Description	RW	Default
0	EnIGMPsnooping	Enable IGMP Snooping. The switch controller features an ASIC-based auto IGMP v1 snooping function. No software support is required. When enabled, the switch can automatically snoop IGMP packets and build up an IP multicast address table. The discovered IP multicast Router port will be indicated in the 'IP Multicast Router Port Discovery Register'. 0: Disable IGMP snooping (Default) 1: Enable IGMP snooping	RW	0
15:1	Reserved			

11.11.6. 0x0309H: IP Multicast Router Port Discovery Register (32 bits)

Table 81. 0x0309H: IP Multicast Router Port Discovery Register (32 bits)

Bits	Name	Description	RW	Default
23:0	IPMRouterDISC[23:0]	IP Multicast Router Ports Discovery Result. This is a bit map that indicates which port is an IP Multicast Router port. IPMRouterDISC[15:0] maps to port 15 ~ 0 Bit [22]: Gigabit Port control bit Bit [23]: MII Port control bit 0: Normal port (Default) 1: IP multicast Router port	R	0
31:24	Reserved			

11.11.7. 0x030BH: VLAN Control Register

Table 82. 0x030BH: VLAN Control Register

Bits	Name	Description	RW	Default
0	EnHomeVlan	Enable VLAN Function. When the VLAN function is enabled, the power on default VLAN topology is 24 Home VLANs for non-EEPROM environments. The VLAN topology can be configured by Port VLAN Configuration Registers. 0: Disable VLAN (Default) 1: Enable VLAN	RW	0 HW pin. EnHomeVLAN

Bits	Name	Description	RW	Default
1	EnUCleaky	Unicast Packet Inter-VLAN Leaky Control. Enables inter-VLAN communication for unicast forwarding packets. Normally, inter-VLAN packet switching is not valid. The RTL8318P supports a control bit to enable inter-VLAN communication in the switch without an external router. 0: Disable (Default) 1: Enable	RW	0
2	EnARPleaky	ARP broadcast Packet Inter-VLAN Leaky Control. Enables inter-VLAN communication for ARP broadcast packet forwarding. 0: Disable (Default) 1: Enable	RW	0
3	EnIPMleaky	IP Multicast Packet Inter-VLAN Leaky Control. Enables inter-VLAN communication for ARP broadcast packet forwarding. 0: Disable (Default) 1: Enable	RW	0
4	En8021Qaware	Enable 802.1Q VLAN tag aware. If 802.1Q VLAN aware, the switch supports the ability to identify the VLAN ID from the VLAN tag. Reset to force the switch to ignore the VLAN tag header and classify the VLAN only by the PVID. 0: Disable 802.1Q VLAN aware (Default) 1: Enable 802.1Q VLAN aware	RW	0
5	EnIR_TagAdmit	Ingress Rule for Acceptable frame types control. If this parameter is set to 'Admit only VLAN-Tagged Frames', any frames received on that port that carry no VID (i.e., Untagged Frames or Priority-Tagged Frames) are discarded. If this parameter is set to 'Admit all Frames', all incoming Priority-Tagged and Untagged Frames are associated with a VLAN by the ingress rule on the receiving port. 0: Admit all Frames (Default) 1: Admit only VLAN-Tagged Frames	RW	0
6	EnIR_MembSet	Ingress Rule for Ingress Filtering control. If the Enable Ingress Filtering parameter 'EnIR_MembSet' is set, then all frames received on a port whose VLAN classification does not include that port in its member set shall be discarded. 0: Disable ingress member set Filtering (Default) 1: Enable ingress member set filtering	RW	0
15:7	Reserved			

11.11.8. 0x030C~0x0317H: Port VLAN ID Assignment Index Register 0~11

For Port(2n), and Port(2n+1) the register is defined as follows: where n=0, 1, 2, …6,7, and 11 (Addr: 0x030CH + n).

Table 83. 0x030C~0x0317H: Port VLAN ID Assignment Index Register 0~11

Bits	Name	Description	RW	Default
7:0	P(2n)_VIDIndex[7:0]	Port(2n) VID assignment Index. Bit[4:0]: Port VID assignment index. Use the index value as the offset to map to the VLAN configuration table to get a 12-bit Port VLAN ID. Bit[7:5]: Reserved	RW	n
15:8	P(2n+1)_VIDIndex[7:0]	Port(2n+1) VID assignment Index. Bit[4:0]: Port VID assignment index. Use the index value as the offset to map to the VLAN configuration table to get a 12-bit Port VLAN ID. Bit[7:5]: Reserved	RW	2n+1

11.11.9. 0x0319~0x031BH: VLAN Output Port Priority-Tagging Control Register 0, 1, 2

For Port(8n), Port(8n+1), …. ~ Port(8n+7) the register(0x0319~0x031A) is defined as follows: n=0, 1

For the Gigabit port, the function is controlled by register 0x031B [13:12]

For the MII port, the function is controlled by register 0x031B [15:14]

Table 84. 0x0319~0x031BH: VLAN Output Port Priority-Tagging Control Register 0, 1, 2

Bits	Name	Description	RW	Default
1:0	P(8n)_PriTagCtl[1:0]	Port(8n) VLAN Output priority Tag/Untag Control. 00: Remove the VLAN tag from a tagged frame 01: Insert priority tag into an untagged high-priority frame (set priority field: 7, VID field: 0 for high priority frame) 10: Insert priority tag into all untagged frames. (set priority field: 7, VID field: 0 for high priority frame; set priority field: 0, VID field: 0 for low priority frame) 11: Don't touch (Don’t modify the packet) (Default)	RW	11
3:2	P(8n+1)_PriTagCtl[1:0]	Port(8n+1) VLAN Output priority Tag/Untag Control.	RW	11
5:4	P(8n+2)_PriTagCtl[1:0]	Port(8n+2) VLAN Output priority Tag/Untag Control.	RW	11
7:6	P(8n+3)_PriTagCtl[1:0]	Port(8n+3) VLAN Output priority Tag/Untag Control.	RW	11
9:8	P(8n+4)_PriTagCtl[1:0]	Port(8n+4) VLAN Output priority Tag/Untag Control.	RW	11
11:10	P(8n+5)_PriTagCtl[1:0]	Port(8n+5) VLAN Output priority Tag/Untag Control.	RW	11
13:12	P(8n+6)_PriTagCtl[1:0]	Port(8n+6) VLAN Output priority Tag/Untag Control.	RW	11
15:14	P(8n+7)_PriTagCtl[1:0]	Port(8n+7) VLAN Output priority Tag/Untag Control.	RW	11

11.12. 0x031D~0x037CH: VLAN Table Configuration Register

Each VLAN configuration entry requires three 16-bit registers. There are 32 VLAN configuration entries in the VLAN table. The VLAN configuration entry is combined with three registers: VLAN_Entry_Configuration_0, 1, 2. For VLAN m, its format is defined as follows: m=0, 1, 2, …. 31.

11.12.1. Register VLAN(m)_Entry_Configuration_0 (Addr: (0x031DH+3m))

Table 85. Register VLAN(m)_Entry_Configuration_0 (Addr: (0x031DH+3m))

Bits	Name	Description	RW	Default
15:0	VLAN(m)_PM[15:0]	VLAN (entry m) Port Member, 24-bit map (bit 0~15). Bit value 0: Port is not a member of the VLAN Bit value 1: Port is a member of the VLAN	RW	-

11.12.2. Register VLAN(m)_Entry_Configuration_1 (Addr: (0x031DH+3m+1))

Table 86. Register VLAN(m)_Entry_Configuration_1 (Addr: (0x031DH+3m+1))

Bits	Name	Description	RW	Default
7:0	VLAN(m)_PM[23:22]	VLAN(m) Port Member 24-bit map (bit 22~23). Bit value 0: Port is not a member of the VLAN Bit value 1: Port is a member of the VLAN	RW	-
15:8	Reserved			

11.12.3. Register VLAN(m)_Entry_Configuration_2 (Addr: (0x031DH+3m+2))

Table 87. Register VLAN(m)_Entry_Configuration_2 (Addr: (0x031DH+3m+2))

Bits	Name	Description	RW	Default
11:0	VLAN(m)_VID[11:0]	VLAN(m) VID[11:0] bit 11~0. Each VLAN must be assigned a 12-bit VID.	RW	0
15:12	Reserved			

11.13. 0x037D~0x037EH: Insert Per-Port VID (PVID) Enabling Register

11.13.1. 0x037D: Insert Per-Port VID (PVID) Enabling Register 0 (P15~P0)

Table 88. Insert Per-Port VID (PVID) Enabling Register 0

Bits	Name	Description	RW	Default
15:0	InsPVID_0[15:0]	Enables per-port insert PVID function (P15-P0). 0: Disable (default) 1: Enable	RW	0

11.13.2. 0x037E: Insert Per-Port VID (PVID) Enabling Register 1 (Gigabit and MII ports)

Table 89. Insert Per-Port VID (PVID) Enabling Register 1

Bits	Name	Description	RW	Default
7:6	InsPVID_1[7:6]	Enables per-port insert PVID function (Gigabit and MII port) Bit [6]: Gigabit Port control bit Bit [7]: MII Port control bit 0: Disable (default) 1: Enable	RW	0
15:8	Reserved			

11.14. QoS Configuration Register

11.14.1. 0x0400H: QoS Control Register

Table 90. 0x0400H: QoS Control Register

Bits	Name	Description	RW	Default
0	EnDSPri	Enable TCP/IP TOS/DS (DiffServ) based Priority QoS. 0: Disabled (Default) 1: Enabled When enabled, the priority definition is defined as follows: High Priority: If TOS/DS[0:5]: (EF) '101110'; (AF) '001010', '010010', '011010', '100010'; (Network Control) "11x000' Low Priority: TOS/DS = Other codepoint values Note 1: The DS[0:5] bit location is equal to the mapping of TOS[0:5] ={precedence[2:0], Delay, Throughput, Reliability}. *Note 2: DS=Differentiated Services, EF= Expected Forwarding, AF= Assured Forwarding.*	RW	0
1	En8021pPri	Enable 802.1p VLAN Tag Based Priority QoS Function. 0: Disable (Default) 1: Enable	RW	0
2	EnFCAutoOff	Enable Flow Control Ability Auto Turn Off for QoS. Enabled: Enables auto turn off of a port's queue flow control ability for 1~2 seconds whenever the port receives a high priority frame. The flow control ability of this port is re-enabled when no high priority frames are received at this port during a 1~2 second period. Disabled: When EnFCAutoOff is disabled, the flow control ability of this port for any packet will be enabled as it was set. 0: Disabled (Default) 1: Enabled	RW	0
4:3	QWEIGHT[1:0]	Weighted round robin ratio setting of priority queue. The frame service rate of High-pri queue to Low-pri queue is: 00: 4:1 (Default) 01: 8:1 10: 16:1 11: High priority queue first always	RW	00
15:5	Reserved			

11.14.2. 0x0401: Port Priority Configuration Register 0

Table 91. 0x0401: Port Priority Configuration Register 0

Bits	Name	Description	RW	Default
15:0	PortPriCfg[15:0]	Port-based Priority setting (Port0 ~ Port15). Sets the priority QoS based on the physical port. If a port is set as a high priority port, all packets received from that port will be treated as high priority packets. Bit value 1: Sets that port as a high priority port Bit value 0: Sets that port as a low priority port *Note: Ports 0~15 map to bits 0~15.*	RW	0

11.14.3. 0x0402: Port Priority Configuration Register 1

Table 92. 0x0402: Port Priority Configuration Register 1

Bits	Name	Description	RW	Default
5:0	Reserved			
7:0	PortPriCfg[7: 6]	Port based Priority setting (Gigabit Port and MII Port). Sets the priority QoS based on the physical port. If a port is set as a high priority port, all packets received from that port will be treated as high priority packets. Bit value 1: Sets that port as a high priority port Bit value 0: Sets that port as a low priority port	RW	0
15:8	Reserved			

11.15. PHY Access Control Register

11.15.1. 0x0500H: PHY Access Control Register

Table 93. 0x0500H: PHY Access Control Register

Bits	Name	Description	RW	Default
4:0	REG_addr	PHY Register address setting for the PHY Access command.	RW	0
9:5	PHY_ID[4:0]	PHY ID (PHY address) setting for the PHY Access command. RTL8318P connected PHY ID is fixed as: Fast Ethernet Port0 ~ 15. PHY ID: 16,17, …, 30, 31. Gigabit Port. PHY ID: 2 MII Port. PHY ID:5.	RW	0
13:10	Reserved			0
14	PHY_RW	PHY Access Command. 0: PHY Access Read command (Default) 1: PHY Access Write command	RW	0
15	PHYCmdExeSta	PHY Access Command Execution Status. 0: Idle (Default) 1: Busy	R	0

11.15.2. 0x0501H: PHY Access Write Data Register

Table 94. 0x0501H: PHY Access Write Data Register

Bits	Name	Description	RW	Default
15:0	PHY_WD[15:0]	PHY Access Write Out Data (16 bits).	RW	0

11.15.3. 0x0502H: PHY Access Read Data Register

Table 95. 0x0502H: PHY Access Read Data Register

Bits	Name	Description	RW	Default
15:0	PHY_RD[15:0]	PHY Access Read In Data (16 bits).	R	0

11.16. Port Control Register

11.16.1. 0x0607H: Global Port Control Register

Table 96. 0x0607H: Global Port Control Register

Bits	Name	Description	RW	Default
0	DisFDFC ($\overline{\text{EnFDFC}}$)	Disable Full Duplex Flow Control (802.3x PAUSE ability). This control bit will be applied to the switch only when a software reset is sent to the switch. This function can also be directly controlled by PHY register access through the PHY Access Control Register 0: Enable 802.3x Pause ability (Default) 1: Disable 802.3x Pause ability	RW	0 HW pin: EnFDFC
1	DisBKP ($\overline{\text{EnBKP}}$)	Globally Disable Half Duplex Back Pressure Flow Control Ability. Set to globally disable the back pressure flow control ability of all ports. 0: Enable back pressure flow control ability (Default) 1: Disable back pressure flow control ability	RW	0 HW pin. EnBKP
2	DisBCSFC	Disable Broadcast Packet Strict Flood Control. This control function is used under 802.3x flow control mode. Strict flood mode will drop broadcast packets (DA: FF-FF-FF-FF-FF-FF) if any destination port member is congested. Loose flood mode allows broadcast packets to be flooded to all non-congested ports. 0: Enable Broadcast Packet Strict Flood (Strict flood mode) (default) 1: Disable Broadcast Packet Strict Flood (Loose flood mode)	RW	0 HW pin. DisBCSFC
3	DisIPMCFC	Disable IP Multicast Packet Strict Flood Control. This control function is used under 802.3x flow control mode. Strict flood mode will drop IP Multicast packets (DA: 01-00-5E-XX-XX-XX) if any destination port member is congested. Loose flood mode allows IP multicast packets to be flooded to all non-congested ports. 0: Disable IP Multicast Packet Strict Flood (Loose flood mode) (default) 1: Enable IP Multicast Packet Strict Flood (Strict flood mode)	RW	0
4	DisBRDCTRL ($\overline{\text{EnBRDCTRL}}$)	Disable Broadcast Storm Filtering Control. Set to disable the broadcast storm filtering control function. 1: Disable Broadcast storm filtering control (Default) 0: Enable Broadcast storm filtering control	RW	1 HW pin: EnBRDCTRL
15:5	Reserved			

11.16.2. 0x0608H: Port Disable Control Register 0

Table 97. 0x0608H: Port Disable Control Register 0

Bits	Name	Description	RW	Default
15:0	PortDisable[15:0]	Port Enable/Disable Control for ports 0~15. Bit value 0: Port enable Bit value 1: Port disable When disabled, the port will disable packet transmission and reception except for Realtek Remote Control Packets. *Note: Ports 0~15 map to bits 0~15.*	RW	0

11.16.3. 0x0609H: Port Disable Control Register 1

Table 98. 0x0609H: Port Disable Control Register 1

Bits	Name	Description	RW	Default
5:0	Reserved			
7:6	Gigabit Port and MII port disable	Port Enable/Disable Control for Gigabit and MII ports. Bit value 0: Port enable Bit value 1: Port disable When disabled, the port will disable packet transmission and reception except for Realtek Remote Control Packets. *Note: Gigabit port and MII port map to bit 7 and bit 6.*	RW	0
15:8	Reserved			

11.16.4. 0x060AH~0x0611, 0x0615. Port Property Configuration Register 0 ~ 11

For Port(2n) and Port(2n+1) the Port Properties are defined as follows: n = 0, 1, ,. …,7, 11 (Addr: 0x060AH +n); where n=0~7 for Fast Ethernet ports, n=11 for gigabit port and MII port.

Table 99. 0x060AH~0x0611,0x0615. Port Property Configuration Register 0 ~ 11

Bits	Name	Description	RW	Default
7:0	P(2n)_Property[7:0]	Port(2n) Port Property configuration. Bit [4:0]: Media Capability[4:0]= (1000F, 100F, 100H, 10F, 10H).(1000F only for Gigabit Port) Bit [5]: Pause ability (1: Enable). Bit [6]: AsyPause ability (Asynchronous Pause) (1. enable) Bit [7]: Enable Auto Negotiation (1: Enable).	RW	100M. 0xAF
15:8	P(2n+1)_Property[7:0]	Port(2n+1) Port property configuration. Bit [3:0]: Media Capability[3:0]= {100F, 100H, 10F, 10H}. Bit [5]: Pause ability (1: Enable). Bit [6]: AsyPause ability (Asynchronous Pause) (1: Enable). Bit [7]: Enable Auto Negotiation (1: Enable).	RW	100M. 0xAF

Note: A configuration update of these registers requires a software reset (via write Reg. 0x0000 bit 0 =1) to force the configuration to be written to the PHY register and restart the auto-negotiation process.

11.16.5. 0x0619H~0x0620,0x0624. Port Link Status Register 0 ~ 7, 11

For Port(2n) and Port(2n+1) the Port Properties are defined as follows:
(n: 0,1,2,. …, 7, 11) (Addr: 0x0619H +n), where n=0~7 for Fast Ethernet ports, n=11 for gigabit port and MII port.

Table 100. 0x0619H~0x0625. Port Link Status Register 0 ~ 11

Bits	Name	Description	RW	Default
7:0	P(2n)_LinkStatus[7:0]	Port (2n) Port Link Status. Bit [1:0]: Link speed[1:0]: 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: NA. Bit [2]: Full duplex: 0: Half duplex 1: Full duplex Bit[3]: Reserved. Bit [4]: Link up: 0: Link down 1: Link up Bit [5]: Flow control (back pressure or 802.3x): For ports 0~15 (Fast Ethernet ports) and MII port. Defined as Pause ability. For Gigabit ports. Defined as TX Pause ability. In half duplex mode. Defined as back pressure ability. 0: Flow control disabled 1: Flow control enabled Bit [6]: AsyPause ability (Asymmetric Pause): For ports 0~15 (Fast Ethernet ports) and MII port : Don't Care. For Gigabit ports. Defined as RX Pause ability. In half duplex mode. Don't Care. 0: Flow control disabled 1: Flow control enabled Bit [7]: Enable Auto Negotiation (AN): 0: Disable AN 1: Enable AN	R	0

Bits	Name	Description	RW	Default
15:8	P(2n+1)_LinkStatus[7:0]	Port(2n+1) Port Link Status. Bit [1:0]: Link speed[1:0]: 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: NA Bit [2]: Full duplex: 0: Half duplex 1: Full duplex Bit[3]: Reserved. Bit [4]: Link up: 0: Link down 1: Link up Bit [5]: Flow control (back pressure or 802.3x): For ports 0~15 (Fast Ethernet ports) and MII port. Defined as Pause ability. For Gigabit ports. Defined as TX Pause ability. In half duplex mode. Defined as back pressure ability. 0: Flow control disabled 1: Flow control enabled Bit [6]: AsyPause ability (Asymmetric Pause): For ports 0~15 (Fast Ethernet ports) and MII port: Don't Care. For Gigabit ports. Defined as RX Pause ability. In half duplex mode. Don't Care. 0: Flow control disabled 1: Flow control enabled Bit [7]: Enable Auto Negotiation (AN): 0: Disable AN 1: Enable AN	R	0

12. MIB Counter Registers

12.1. 0x0700H~0x0707H, 0x070BH: Port MIB Counter Object Selection Register 0~7, 11

For Port(2n), Port(2n+1), the Port MIB Counter Object Selection Register is defined as follows:

n = 0, 1, 2, …7, 11) (Addr=0x0700H +n). where n=0~7 for Fast Ethernet ports, n=11 for gigabit port and MII port.

Table 101. 0x0700H~0x070BH: Port MIB Counter Object Selection Register 0~11

Bits	Name	Description	RW	Default
1:0	P(2n)CNT1_MIBS [1:0]	Port(2n) Counter_1 MIB Object Selection. P(2n)CNT_1_MIBS [1:0] 00: MIB object: RX byte count 01: MIB object: RX packet count (Default) 10: MIB object: CRC error packet count 11: MIB object: Collision packet count RX byte count. This counter is incremented once for every data byte of a received and forwarded packet (includes both good and bad packets). RX packet count. This counter is incremented once for every received and forwarded packet (includes both good and bad packets).	RW	01
3:2	P(2n)CNT2_MIBS [1:0]	Port(2n) Counter_2 MIB Object Selection. P(2n)CNT_2_MIBS [1:0] 00: MIB object: TX byte count 01: MIB object: TX packet count (Default) 10: MIB object: CRC error packet count 11: MIB object: Collision packet count TX byte count. This counter is incremented once for every data byte of a transmitted packet (includes both good and bad packets). TX packet count. This counter is incremented once for every transmitted packet (includes both good and bad packets).	RW	01

Bits	Name	Description	RW	Default
5:4	P(2n)CNT3_MIBS [1:0]	Port(2n) Counter_3 MIB Object Selection P(2n)CNT_3_MIBS [1:0] 00: MIB object: Drop byte count 01: MIB object: Drop packet count (Default) 10: MIB object: CRC error packet count 11: MIB object: Collision packet count Drop packet count. This counter is incremented once for every drop of a received packet. Packet drop events could be due to undersize, oversize, CRC error, lack of resources, local packet, point-to-point control packet (ex. Pause packet, LACP packet, including RRCP® packets). CRC error packet count. This counter is incremented once for every received packet with a valid length but with a CRC error. Collision packet counter. This counter is incremented once for every collision event detected.	RW	01
7:6	P(2n+1)CNT1_MIBS [1:0]	Port(2n+1) Counter_1 MIB Object Selection.	RW	01
9:8	P(2n+1)CNT2_MIBS [1:0]	Port(2n+1) Counter_2 MIB Object Selection.	RW	01
11:10	P(2n+1)CNT3_MIBS [1:0]	Port(2n+1) Counter_3 MIB Object Selection.	RW	01

12.2. 0x070DH ~0x071CH, 0x0723, 0x0724H: Port MIB Counter 1 Register (RX Counter) (32 bits)

The MIB counters are 32-bit counters. After power on reset, the counters are all reset to 0. A read access of the MIB counter will NOT reset the counter to 0. When a MIB counter MIB object is changed, then the counter will be reset to 0 and the count will restart.

The time before the next read of the same counter should not be longer than the counter's timeout. The timeout of the 32-bit MIB counter depends on the object type and the port speed, and is calculated as follows:

Packet counter timeout is calculated based on 64-byte packets and byte counter timeout is calculated based on 1518 byte packets).

Table 102. MIB Counter Timeout

Port Speed	MIB Object Type	MIB Counter Timeout (Sec.)
1000Mbps	Packet count	2886
	Byte count	34
100Mbps	Packet count	28862
	Byte count	348
10Mbps	Packet count	288621
	Byte count	3481

12.2.1. For Port(n) MIB Counter 1 Register (32-bit). n=0, 1, 2, …15, 22, 23 (Addr: 0x070DH+n).

For Port(n) MIB Counter 1 Register (32-bit). n=0, 1, 2, …15, 22, 23 (Addr: 0x070DH+n) (where n=0~15 for Fast Ethernet ports, n=22, 23 for gigabit port and MII port)

Table 103. 0x070DH ~0724H: Port MIB Counter 1 Register (RX Counter) (32 bits)

Bits	Name	Description	RW	Default
31:0	Port(n)_MIB_CNT_1[31:0]	Port(n) MIB Counter_1[31:0]	R	0

12.2.2. 0x0727~0x0736H, 0x073D, 073EH: Port MIB Counter 2 Register (TX Counter) (32-bits)

For Port(n) MIB Counter 2 Register (32-bit): n = 0, 1, 2, … 15, 22, 23 (Addr: 0x0727H+n). where n=0~7 for Fast Ethernet ports, n=11 for gigabit port and MII port

Table 104. 0x0727~073EH: Port MIB Counter 2 Register (TX Counter) (32 bits)

Bits	Name	Description	RW	Default
31:0	Port(n)_MIB_CNT_2[31:0]	Port(n) MIB Counter_2[31:0]	R	0

12.2.3. 0x0741~0x0750, 0x0757, 0x0758H: Port MIB Counter 3 Register (Diagnostic Counter) (32-bits)

For Port(n) MIB Counter 3 Register (32-bit): n = 0, 1, 2, … 15, 22, 23 (Addr: 0x0741H+n).

Table 105. 0x0741~0758H: Port MIB Counter 3 Register (Diagnostic Counter) (32 bits)

Bits	Name	Description	RW	Default
31:0	Port(n)_MIB_CNT_3[31:0]	Port(n) MIB Counter_3[31:0]	R	0

13. Characteristics

13.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device or which may affect device reliability. All voltages are specified reference to GND unless otherwise specified.

Table 106. Absolute Maximum Ratings

Parameter	Min	Max	Units
Storage Temperature	-10	+125	°C
DVDD, RVDD, AVDD Supply Referenced to GND	GND-0.3	+3.63	V
VDD Supply Reference to GND	GND-0.3	+1.98	V
Digital Input Voltage	GND-0.3	DVDD+0.3	V

13.2. Operating Range

Table 107. Operating Range

Parameter	Min	Typical	Max	Units
Ambient Operating Temperature	0	-	70	°C
3.3V Supply Voltage Range (RVDD, DVDD, AVDD)	3.15	3.3	3.45	V
1.8V Supply Voltage Range (VDD)	1.71	1.8	1.89	V

13.3. DC Characteristics

Supply Voltage VDD: 3.3V ± 5%.

Table 108. DC Characteristics

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Power Supply Current	Icc	17FE, 1Gb port wire-speed traffic load 17FE, 1Gb port all idle			280 170	mA
Total Power Consumption	PS	17FE, 1Gb port wire-speed traffic load 17FE 1Gb port all idle			924 561	mW
TTL Input High Voltage	V_{ih}		2.0			V
TTL Input Low Voltage	V_{il}				0.8	V
TTL Input Current	I_{in}		-10		10	µA
TTL Input Capacitance	C_{in}			2.9		pF
Output High Voltage	V_{oh}		2.6		3.6	V
Output Low voltage	V_{ol}		0		0.4	V

13.4. AC Characteristics

13.4.1. PHY Management (SMI) Timing

Table 109. PHY Management (SMI) Timing

Symbol	Description	Minimum	Typical	Maximum	Units
t1	MDC clock period	-	1360	-	ns
t2	MDC high level width	-	680	-	ns
t3	MDC low level width	-	680	-	ns
t4	MDIO to MDC rising setup time (Write Bits)		680	-	ns
t5	MDIO to MDC rising hold time (Write Bits)		680	-	ns
t6	MDC to MDIO delay (Read Bits)	20	-	-	ns
t7	MDC/MDIO actives from RST# deasserted	-	45	-	ms

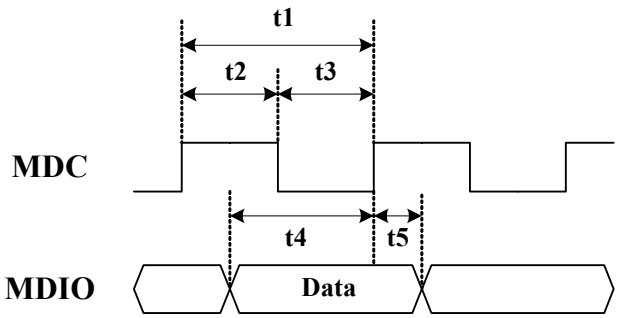


Figure 16. MDC/MDIO Write Timing

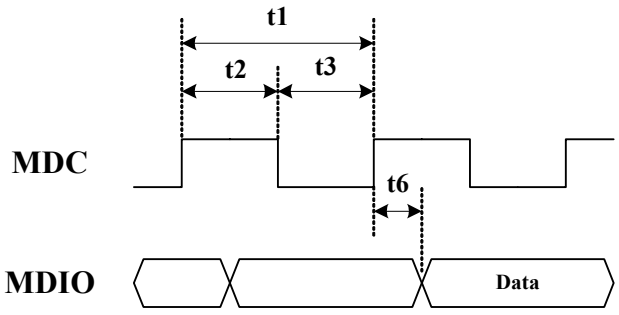


Figure 17. MDC/MDIO Read Timing

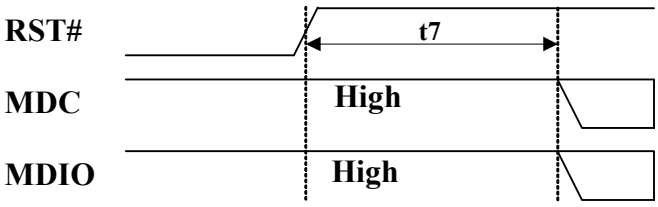


Figure 18. MDC/MDIO Reset Timing

13.4.2. SMII Transmit Timing

Table 110. PHY Management (SMI) Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_opd_txd_smii	REFCLK rising edge to TXD (SYNC) delay.	2	4	5	ns

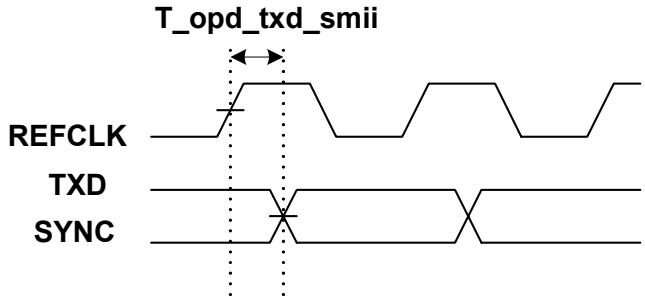


Figure 19. SMII Transmit Timing

13.4.3. SMII Receive Timing

Table 111. SMII Receive Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_ipsu_rxd_smii	RXD setup time to REFCLK.	2			ns
T_iphd_rxd_smii	RXD hold time from REFCLK.	1.5			ns

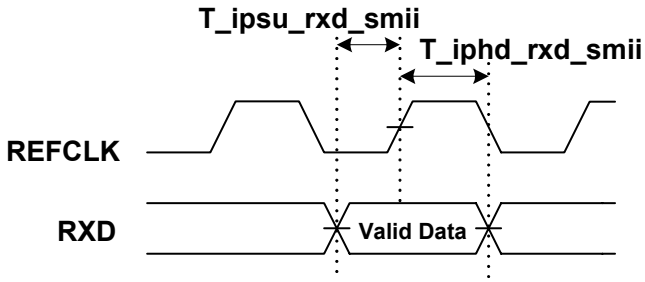


Figure 20. SMII Receive Timing

13.4.4. GMII Transmit Timing

Table 112. GMII Transmit Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_opd_txd_gmii	GxTX_CLK rising edge to TXD delay.	1.2	2.5	4	ns

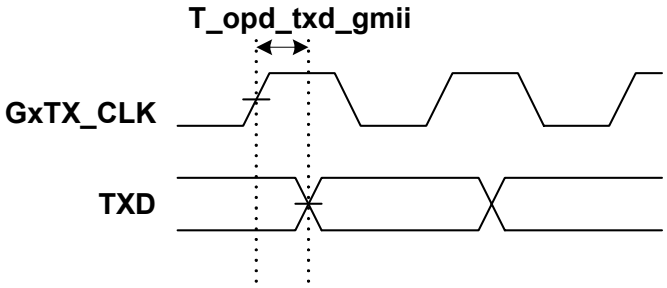


Figure 21. GMII Transmit Timing

13.4.5. GMII Receive Timing

Table 113. GMII Receive Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_su_rxd_gmii	RXD(RX_DV) setup time to GxRX_CLK.	2.5			ns
T_hd_rxd_gmii	RXD(RX_DV) hold time from GxRX_CLK.	0.5			ns

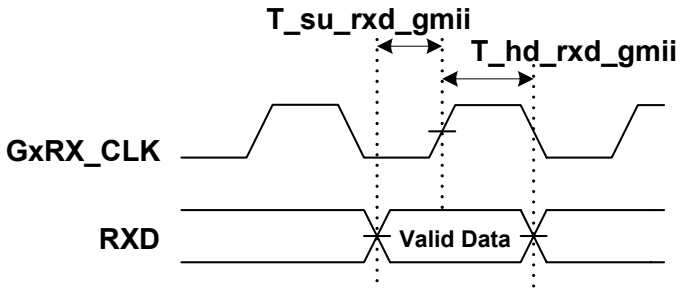


Figure 22. GMII Receive Timing

13.4.6. MII Transmit Timing

Table 114. MII Transmit Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_opd_txd_mii	GxTXC rising edge to TXD delay.	4	7.4	10	ns

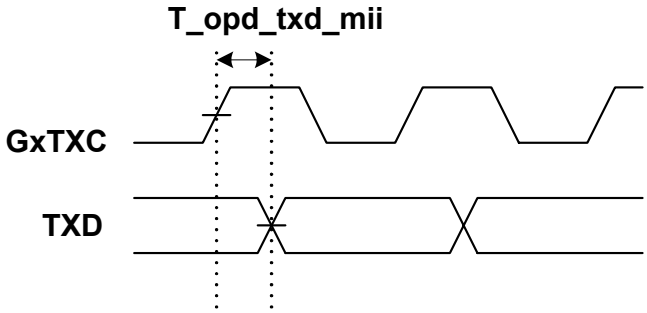


Figure 23. MII Transmit Timing

13.4.7. MII Receive Timing

Table 115. MII Receive Timing

Symbol	Description	Minimum	Typical	Maximum	Units
T_su_rxd_mii	RXD(RX_DV) setup time to GxRXC.	2			ns
T_hd_rxd_mii	RXD(RX_DV) hold time from GxRXC.	1			ns

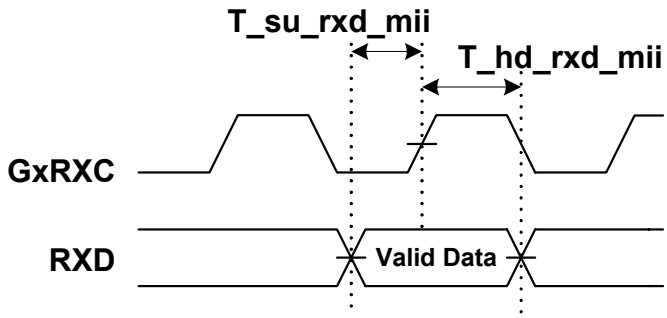


Figure 24. MII Receive Timing

14. Thermal Data

14.1. Thermal Characteristics

Heat generated by the chip causes a temperature rise of the package. If the temperature of the chip (Tj, junction temperature) is beyond the design limits, there will be negative effects on operation and the life of the IC package. Heat dissipation, either through a heat sink or electrical fan, is necessary to provide a reasonable environment (Ta, ambient temperature) in a closed case. As power density increases, thermal management becomes more critical. A method to estimate the possible Ta is outlined below.

Thermal parameters are defined according to JEDEC standard JESD 51-2, 51-6:
θ_{JA} (Thermal resistance from junction to ambient), represents resistance to heat flow from the chip to ambient air. This is an index of heat dissipation capability. A lowerθ_{JA} means better thermal performance.

θ_{JA} = (Tj – Ta) / Ph, where Tj is the junction temperature
Ta is the ambient temperature
Ph is the power dissipation

θ_{JC} (Thermal resistance from junction to case), represents resistance to heat flow from the chip to the package top case. θ_{JC} is important when an external heat sink is attached on the package top.

θ_{JC} = (Tj – Tc) / Ph, where Tj is the junction temperature.

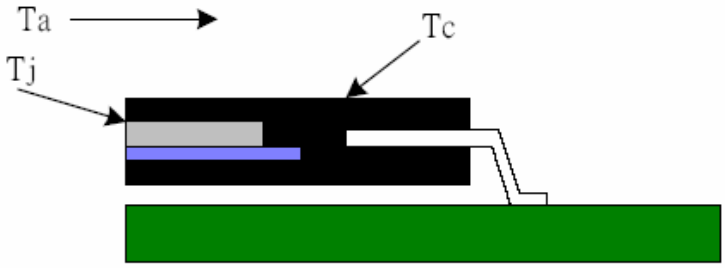


Figure 20. Cross-section of 128-Pin PQFP

14.2. Thermal Operating Range

Table 116. Thermal Operating Range

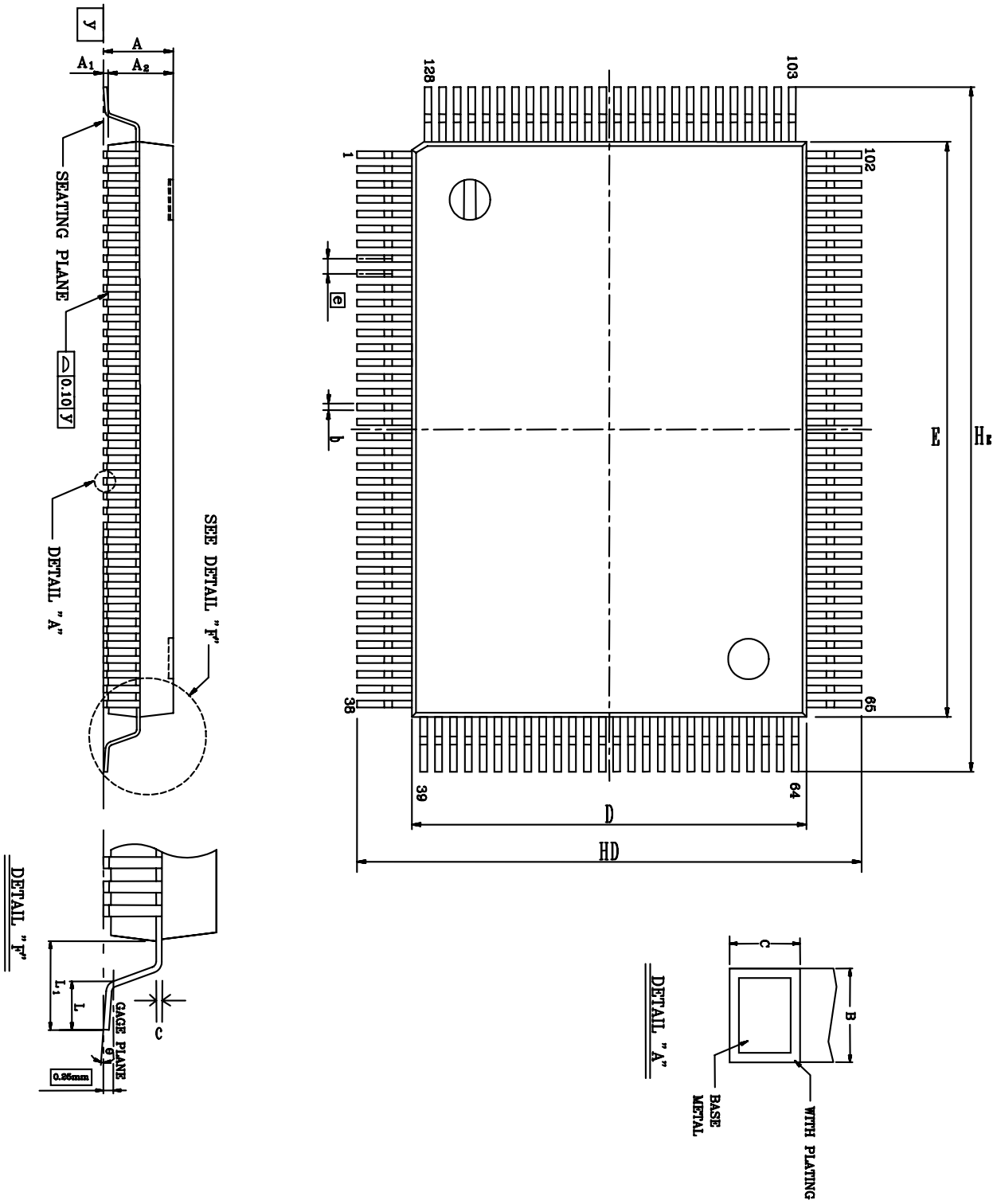
Parameter	SYM	Conditions	Min	Typical	Max	Units
Junction operating Temperature	Tj			25	125	°C
Junction operating Temperature	Ta			25	70	°C

14.3. Thermal Resistance

Table 117. Thermal Resistance

Parameter	SYM	Conditions	Min	Typical	Max	Units
Thermal resistance: junction to ambient	θ_{JA}	2 layer PCB, 0 ft/s airflow		48.5		°C/W
Thermal resistance: junction to case	θ_{JC}	2 layer PCB, 0 ft/s airflow		16.4		°C/W

Mechanical Information



See the Mechanical Dimensions notes on the next page.

14.4. Mechanical Dimensions Notes

Symbol	Dimensions in inches			Dimensions in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.134	-	-	3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. Should be based on final visual inspection.

TITLE: -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	1.2
		PAGE	
CHECK		DWG NO.	Q128 - 1
		DATE	
REALTEK SEMICONDUCTOR CORP.			

15. Ordering Information

Table 118. Ordering Information

Part Number	Package	Status
RTL8318P-LF	PQFP-128 with Lead (Pb)-Free package	Available Now

Note: See page 5 for lead (Pb)-free package identification.

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