RTL8305S
5-PORT 10/100 MBPS SINGLE CHIP SWITCH CONTROLLER

1. Features

- 5-port integrated switch with physical layer and transceiver for 10Base-T and 100Base-TX with
  5-port 10/100M UTP or
  4-port 10/100M UTP + 1-port MII/SNI
- PHY mode MII/SNI interface for router application
- MAC mode MII interface for HomeLAN/100Base-FX application
- 1Mbit internal RAM for packet buffer
- Internal 1K look-up table entries
- 25MHz crystal or OSC input
- Non-blocking wire-speed reception and transmission
- Fully compliant with IEEE 802.3/802.3u
- Supports broadcast storm filtering function
- Support full duplex 802.3x flow control and half duplex back-pressure flow control
- LED indicators for link/activity, speed, full/half duplex and collision
- LEDs blinking upon reset for LED diagnostics
- Unmanaged operation by strapping upon reset
- Power saving with cable detection
- Low power consumption at 3.3V operating voltage
- 128-pin PQFP package

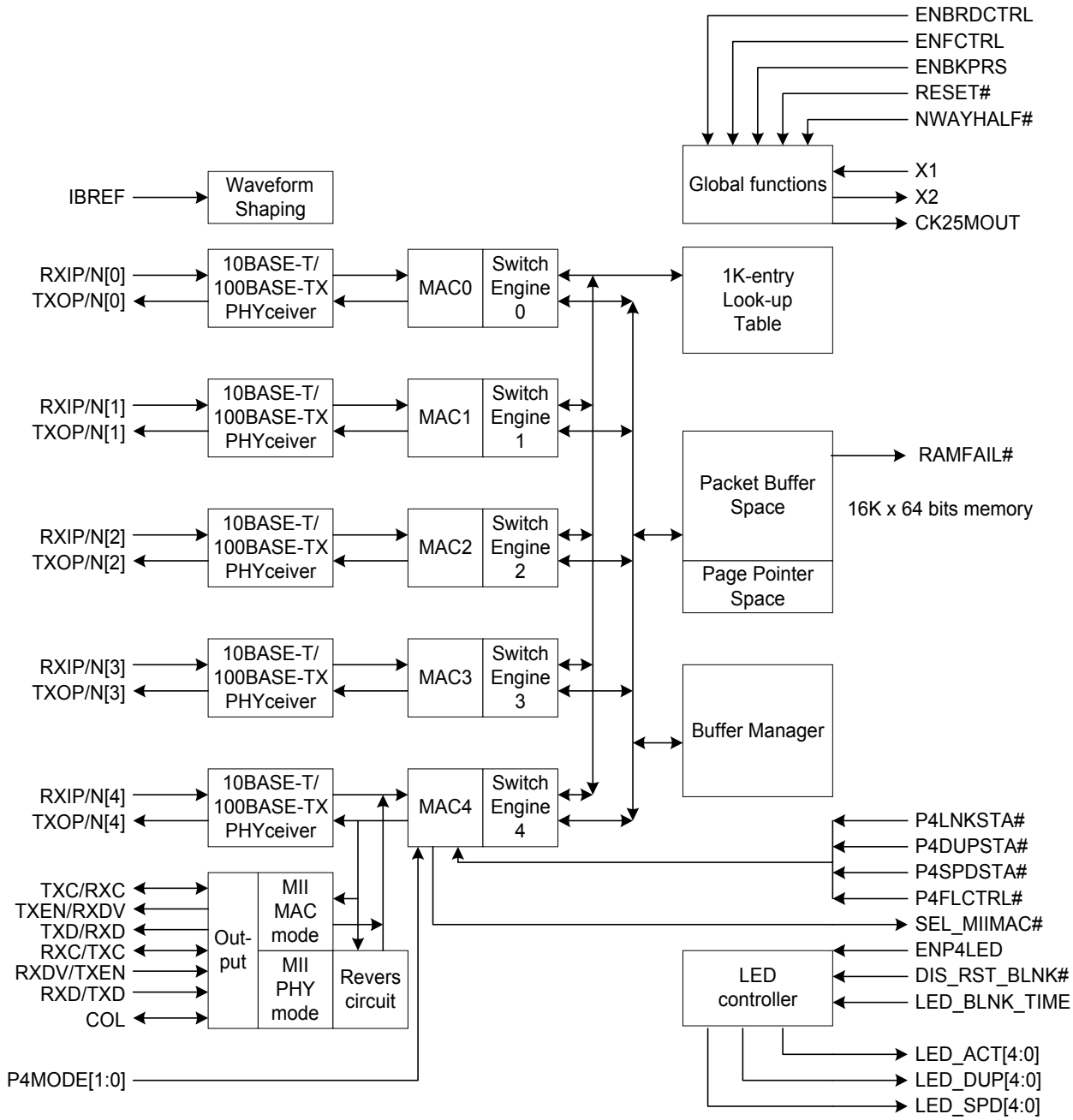
2. General Description

The RTL8305S is a highly integrated layer 2 single chip switch controller which incorporates 5 MACs (Media Access Controller), 5 physical layer transceivers, 1-Mbit SRAM and 1K-entry look-up table into one single chip.

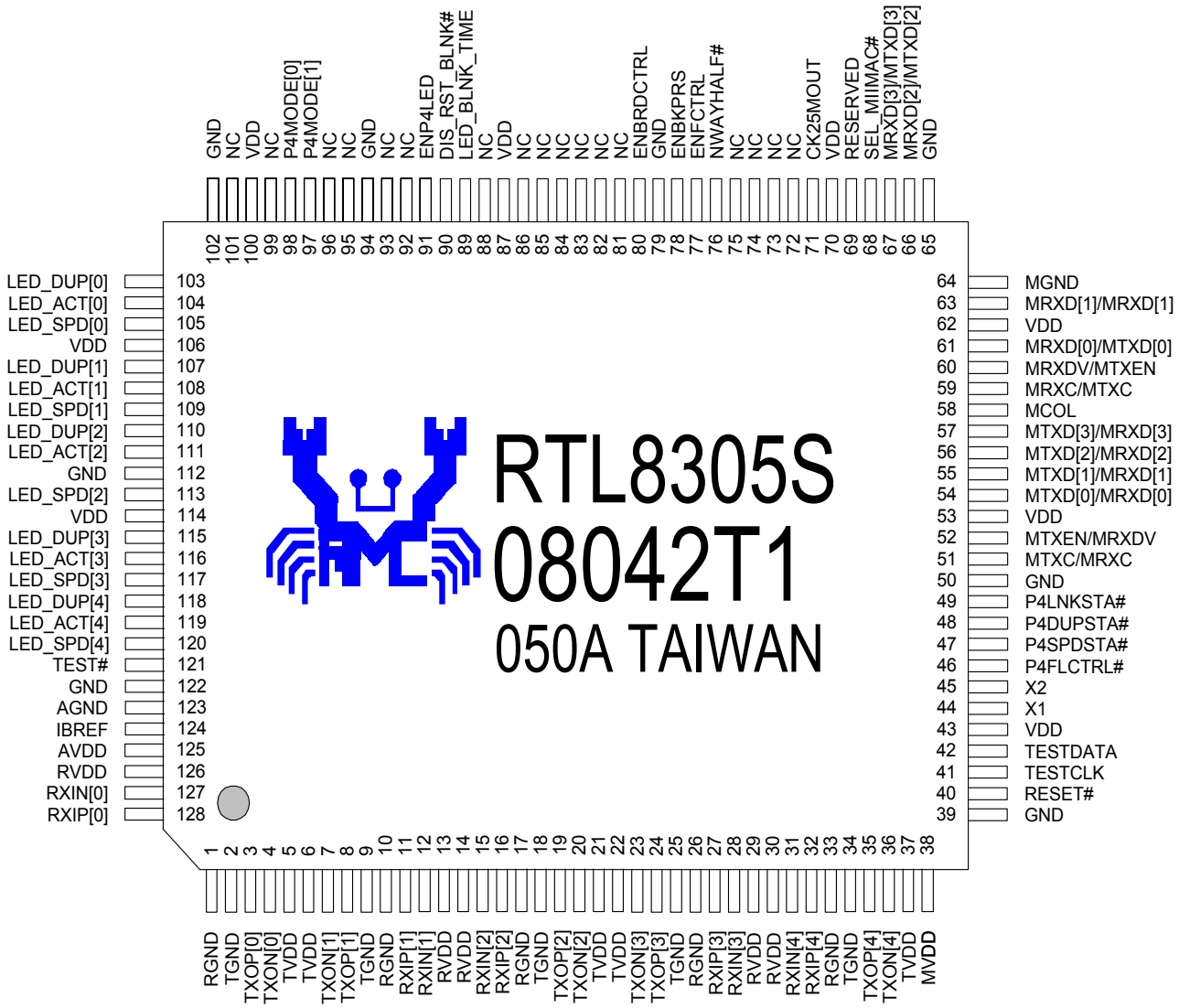
The RTL8305S contains 5 ports, and each one provides support for a 10Base-T (10Mbps) or 100Base-TX (100Mbps) network connection. The fifth port (port 4) can be configured as a MII/SNI to work with a routing engine, HomePHY or a fiber transceiver for a 100Base-FX application. And each operation mode can be easily set up by hardware strapping upon restart or power-on.

The RTL8305S is designed for a stand-alone switch system through hardware strapping upon reset to achieve unmanaged operation and can be easily integrated with xDSL/Cable modem router. With the least peripheral components and using a 25MHz crystal, the RTL8305S has the best system cost structure. The integrated RTL8305S chip benefits from low power consumption and ease of use for SOHO 5-port switch or xDSL/Cable router applications.

3. Block Diagram



4. Pin Assignments



' I ' stands for inputs; 'O' stands for outputs; 'A' stands for analog; 'D' stands for digital

Name	Pin No.	Type	Name	Pin No.	Type
RGND	1	AGND	GND	65	DGND
TGND	2	AGND	MRXD[2]/MTXD[2]	66	I
TXOP[0]	3	AO	MRXD[3]/MTXD[3]	67	I
TXON[0]	4	AO	SEL_MIIMAC#	68	O
TVDD	5	AVDD	RESERVED	69	I
TVDD	6	AVDD	VDD	70	DVDD
TXON[1]	7	AO	CK25MOUT	71	O
TXOP[1]	8	AO	NC	72	
TGND	9	AGND	NC	73	
RGND	10	AGND	NC	74	
RXIP[1]	11	AI	NC	75	
RXIN[1]	12	AI	NWAYHALF#	76	I
RVDD	13	AVDD	ENFCTRL	77	I
RVDD	14	AVDD	ENBKPRS	78	I
RXIN[2]	15	AI	GND	79	DGND
RXIP[2]	16	AI	ENBRDCTRL	80	I
RGND	17	AGND	NC	81	
TGND	18	AGND	NC	82	
TXOP[2]	19	AO	NC	83	
TXON[2]	20	AO	NC	84	
TVDD	21	AVDD	NC	85	
TVDD	22	AVDD	NC	86	
TXON[3]	23	AO	VDD	87	DVDD
TXOP[3]	24	AO	NC	88	
TGND	25	AGND	LED_BLNK_TIME	89	I
RGND	26	AGND	DIS_RST_BLNK#	90	I
RXIP[3]	27	AI	ENP4LED	91	I
RXIN[3]	28	AI	NC,	92	
RVDD	29	AVDD	NC	93	
RVDD	30	AVDD	GND	94	DGND
RXIN[4]	31	AI	NC	95	
RXIP[4]	32	AI	NC	96	
RGND	33	AGND	P4MODE[1]	97	I
TGND	34	AGND	P4MODE[0]	98	I
TXOP[4]	35	AO	NC	99	
TXON[4]	36	AO	VDD	100	DVDD
TVDD	37	AVDD	NC	101	
MVDD	38	DVDD	GND	102	DGND
GND	39	DGND	LED_DUP[0]	103	O
RESET#	40	I	LED_ACT[0]	104	O
TESTCLK	41	I	LED_SPD[0]	105	O
TESTDATA	42	I/O	VDD	106	DVDD
VDD	43	DVDD	LED_DUP[1]	107	O
X1	44	I	LED_ACT[1]	108	O
X2	45	O	LED_SPD[1]	109	O
P4FLCTRL#	46	I	LED_DUP[2]	110	O
P4SPDSTA#	47	I	LED_ACT[2]	111	O
P4DUPSTA#	48	I	GND	112	GND
P4LNKSTA#	49	I	LED_SPD[2]	113	O
GND	50	DGND	VDD	114	DVDD
MTXC/MRXC	51	I/O	LED_DUP[3]	115	O
MTXEN/MRXDV	52	O	LED_ACT[3]	116	O
VDD	53	DVDD	LED_SPD[3]	117	O
MTXD[0]/MRXD[0]	54	O	LED_DUP[4]	118	O
MTXD[1]/MRXD[1]	55	O	LED_ACT[4]	119	O
MTXD[2]/MRXD[2]	56	O	LED_SPD[4]	120	O
MTXD[3]/MRXD[3]	57	O	TEST#	121	O
MCOL	58	I/O	GND	122	DGND
MRXC/MTXC	59	I/O	AGND	123	AGND
MRXDV/MTXEN	60	I	IBREF	124	A
MRXD[0]/MTXD[0]	61,	I	AVDD	125	AVDD
VDD	62	DVDD	RVDD	126	AVDD
MRXD[1]/MTXD[1]	63	I	RXIN[0]	127	AI
MGND	64	DGND	RXIP[0]	128	AI

5. Pin Descriptions

5.1 Media Connection Pins

Pin Name	Pin No.	Type	Description	Default
RXIP[4:0] RXIN[4:0]	11,12,15 16,27,28 31,32,127 128	AI	**Differential Receive Data Input**	
TXOP[4:0] TXON[4:0]	3,4,7,8 19,20,23 24,35,36	AO	**Differential Transmit Data Output**	

5.2 Mode Pins

Pin Name	Pin No.	Type	Description	Default
ENBKPRS	78	I	**Enable Back Pressure:** This pin has no effect on port4 if it is operated as an MII port. 1: Enable (UTP ports only) 0: Disable	**1**
ENFCTRL	77	I	**Enable Flow Control:** The RTL8305S will advertise its ability with flow control during auto-negotiation. This pin has no effect on port4 if it is operated as an MII port. 1: Enable Flow control (UTP ports only) 0: Disable	**1**
ENBRDCTRL	80	I	**Enable Broadcast Control:** This is for the UTP and MII port. 1: Enable 0: Disable	**1**
LED_BLNK_TIME	89	I	**LED Blinking Time:** This pin controls the blinking speed of the activity and collision LEDs. 1: 43ms 0: 120ms	**1**
DIS_RST_BLNK#	90	I	**Disable Reset Blinking:** This pin controls the blinking of LEDs during reset and power up. Set to 0, the LEDs will not blink on reset or power up. 1: Enable 0: Disable	**1**
NWAYHALF#	76	I	**Nway Half Duplex:** This pin advertises Nway ability to the link partner. Setting this pin to 0 will advertise an Nway ability with 10/100 half duplex only. 1: Nway ability supports full duplex 0: Nway ability supports half duplex only	**1**
TEST#	121	O	**Test:** An internal test pin	

5.3 Port4 Related Pins

Pin Name	Pin No.	Type	Description	Default
MRXD[3:0] /MTXD[3:0]	67,66,63 61	I	For MII MAC mode, these pins are MRXD[3:0], MII receive data nibble. For MII PHY mode, these pins are MTXD[3:0], MII transmit data nibble. For SNI PHY mode, MTXD[0] is serial transmit data.	
MRXDV/MTXEN	60	I	For MII MAC mode, this pin represents MRXDV, MII receive data valid. For MII PHY mode, this pin represents MTXEN, MII transmit enable.	
MRXC/MTXC	59	I/O	For MII MAC mode, it is receive clock, MRXC (acts as input). For MII/SNI PHY mode, it is transmit clock, MTXC (acts as output).	
MCOL	58	I/O	For MII MAC mode, this pin represents collision (acts as input) For MII/SNI PHY mode, this pin represents collision (acts as output)	
MTXD[3:0] /MRXD[3:0]	57,56,55 54	O	For MII MAC mode, these pins are MTXD[3:0], MII transmit data nibble. For MII PHY mode, these pins are MRXD[3:0], MII receive data nibble. For SNI PHY mode, MRXD[0] is serial receive data.	
MTXEN/MRXDV	52	O	For MII MAC mode, this pin represents MTXEN, MII transmit enable. For MII PHY mode, this pin represents MRXDV, MII receive data valid.	
MTXC/MRXC	51	I/O	For MII MAC mode, this pin is a transmit clock, MTXC (acts as input). For MII/SNI PHY mode, this pin is a receive clock, MRXC (acts as output).	
P4MODE[1:0]	97,98	I	**Select Port 4 Operating Mode:** 00: SNI PHY mode 01: MII PHY mode 1x: UTP / MII MAC mode	**11**
P4LNKSTA#	49	I	**Port 4 Link Status:** When P4MODE[1]=1 (UTP/MII MAC mode), this pin decides the link status of the MII port. If both UTP and MII MAC are linked OK, UTP has higher priority. When P4MODE[1]=0 (PHY mode), this pin decides link status of Port4.	**1**
P4DPXSTA#	48	I	**Active Low Duplex Status:** 1: Half duplex 0: Full duplex When P4 is operated in UTP mode, this pin has no effect.	**1**
P4SPDSTA#	47	I	**Active Low Speed Status:** 1: 10Mbps 0: 100Mbps This pin must be kept floating for the three applications listed below. This is because the speed is either determined by auto-negotiation or fixed at 1M/10M Hz. 1. For UTP mode, speed is determined by the auto-negotiation procedure. 2. For HomePNA (MII MAC mode), speed is determined by RXC and TXC from HomePHY running at 1Mbps. 3. For SNI PHY mode, speed is dedicated to 10MHz clock rate.	**1**
P4FLCTRL#	46	I	**Active Low Flow Control Enable:** When P4 is operated in UTP mode, this pin has no effect. 1: Disable 0: Enable	**1**
ENP4LED	91	I	**Enable Port 4 LED:** In UTP applications, this pin should be floating to drive the LEDs of port 4. 1: Drive LED pins of port4 0: Tri-state LED pins of port4	**1**
SEL_MIIMAC#	68	O	**Select MII MAC:** When P4MODE[1]=1, this pin indicates whether UTP path or MII MAC path is selected. 1: UTP is selected 0: MII port is selected While P4MODE[1]=1, the RTL8305S supports UTP/MII MAC auto-detect function via the link status of P4 UTP and the status of P4LINKSTA# with priority UTP over MII.	

5.4 LED Pins

Pin Name	Pin No.	Type	Description	Default
LED_ACT[4:0]	119,116 111,108 104	O	Active low (Link + Activity) LED pins.	**1**
LED_DPX[4:0]	118,115 110,107 103	O	Active low (Fullduplex + Collision) LED pins.	**1**
LED_SPD[4:0]	120,117 113,109 105	O	Active low Speed100 LED pins.	**1**

5.5 Power Pins

Pin Name	Pin No.	Type	Description	Default
TVDD	5,6,21 22,37	P	3.3V Analog Transmit Power	
RVDD	13,14,29 30,126	P	3.3V Analog Receive Power	
AVDD	125	P	3.3V Analog Power	
MVDD	38	P	3.3V Internal RAM Power	
VDD	43,53,62 70,87,100 106,114	P	3.3V Digital Power	
RGND	1,10,17 26,33	P	Analog Ground	
TGND	2,9,18 25,34	P	Analog Ground	
AGND	123	P	Analog GND	
MGND	64	P	Internal RAM GND	
GND	39,50,65 79,94,102 112,122	P	Digital GND	

5.6 Miscellaneous Pins

Pin Name	Pin No.	Type	Description	Default
X1	44	I	25MHz crystal or oscillator clock input	
X2	45	O	To crystal input. When using an oscillator this pin should be kept floating.	
CK25MOUT	71	O	25MHz clock output	
RESET#	40	I	Active low reset signal. To complete the reset function, this pin must be asserted for at least 10ms. After reset, about 30ms is needed for the RTL8305S to complete the internal test function and initialization.	
IBREF	124	A	Control transmit output waveform Vpp. This pin should be grounded through a 1.96KΩ resistor.	
TESTCLK	41	I	Test clock	
TESTDATA	42	I/O	Test data	

5.7 Reserved Pins

Pin Name	Pin No.	Type	Description	Default
RESERVED	69	I	This pin is reserved for internal use and should be left floating.	**1**

6. Functional Description

6.1 Introduction

Providing five 10/100 Mbps Ethernet channels and one MII port, the RTL8305S can be configured for either a five port 10/100 Ethernet application or a four 10/100 port Ethernet with an extra MII/SNI port. The MII/SNI port can be connected to an external processor for routing purposes as public area network devices do, referred to as MII/SNI PHY mode, or connected to a HomePNA physical chip or 100Base-FX PHYceiver, referred to as MII MAC mode.

In MII/SNI PHY mode, pins RXC, RXDV, and RXD correspond to TXC, TXEN, and TXD. In MII MAC mode, TXC, TXEN and TXD correspond to RXC, RXDV and RXD.

The frame buffer is composed of 1M bits of built-in memory. The address look-up table for MAC addresses learning/searching consists of 1K direct-mapping entries.

The RTL8305S uses Nway auto-negotiation to complete the UTP port connections of physical links which conform to IEEE 802.3u specifications. IEEE 802.3x full duplex flow control is supported. When operating in half duplex mode, a proprietary back-pressure algorithm is implemented to prevent traditional hub devices from partitioning due to excessive collisions.

The RTL8305S supports non-blocking wire speed forwarding rates and special designs to resolve head-of-line blocking problems and channel-capture problems. A broadcast storm filtering function is also provided for abnormal broadcast traffic issues.

6.2 Switch Core Functional Overview

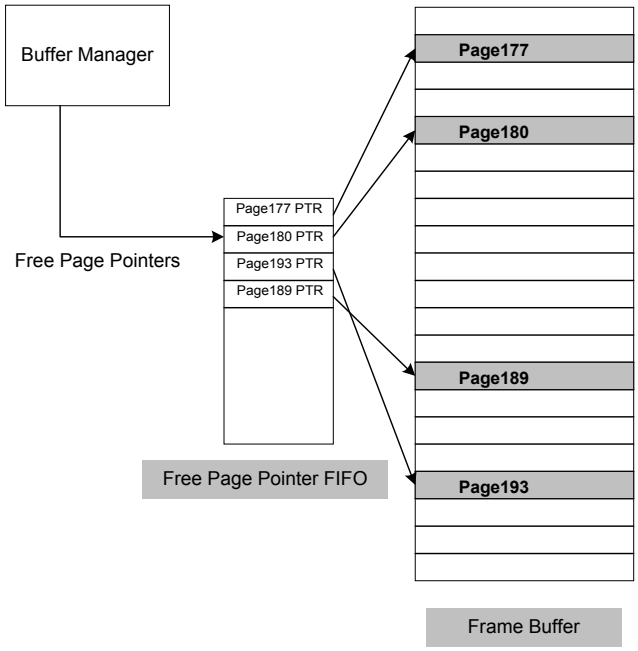
6.2.1 Address Search, Learning and Aging

The RTL8305S contains a full 1K of look-up table entries and uses a direct-mapping scheme to achieve address search and learning.

By extracting the least 10 bits of a destination MAC address to index the 1K-entry look-up table, the RTL8305S can decide where the packet goes. If the searching result indexes to an empty entry, the packet is broadcast to all other ports. On the other hand, the RTL8305S extracts the least 10 bits of a source MAC address to index the 1K-entry look-up table. If the result indexes to an empty entry, it records the source MAC address and related switching information. If the result leads to an occupied entry with different switching information, it updates the entry with the new information. This is referred to as ‘learning.’ The look-up engine will update time stamp information of an entry whenever the corresponding source MAC address appears. If the time information is not updated for a period of time, the entry will be removed, referred to as the aging process. The maximum aging time for the RTL8305S is approximately 300 seconds, and the minimum aging time is approximately 200 seconds.

6.2.2 Buffer Management

The 1M bit embedded memory buffer is divided into a packet buffer, which is used for data buffering, and a page pointer block (PPB), which is used by the buffer manager. The Packet buffer is constructed of approximately 512 256-byte pages. Each page includes 8-bytes of header information, which consists of next page pointer, packet byte count, and 248 bytes of data. The linked pages construct a whole received packet which will be forwarded later according to its destination. The buffer manager gets free page pointers from PPB and releases to each port to provide space for incoming packet buffering. When the buffer manager can not support free page pointers any more, it indicates a buffer full condition and 802.3x flow control or back pressure congestion control is implemented. If no flow control algorithms are activated, packets are dropped.



6.2.3 Data Reception

Each port contains a Receive FIFO for incoming packets, which are from physical medium, and a Free Page Pointer FIFO for packet buffering indexes. Free Page Pointers are obtained from the Buffer Manager. Once a packet is received, it is segmented into 248-byte pieces (as is fit into pages) and then moved into a packet buffer by the Receive DMA Engine with an 8-byte header in every page.

6.2.4 Data Forwarding

Each port contains a Transmit FIFO, a Transmit Free Page Pointer FIFO and a Transmit Start Address Queue. The Transmit Free Page Pointer FIFO stores Free Pages Pointers which have just been released from transmitted packets, and will return these Free Pages to the Buffer Manager for buffering indexes of the next incoming packets. The Transmit Start Address Queue keeps the first page pointer of every egress packet, which is from the transmit command issued by the reception port (source port). The destination ports identify every transmit command on the global bus and receive it if they are the outlets. Finally, the Transmit DMA engine of each port starts the DMA to move the pages (which construct a whole packet) to Transmit FIFO and then to the physical medium. For broadcast packets, it's the duty of the last port which finishes the transmission action last to return the Transmit Free Page Pointers to the Buffer Manager.

6.2.5 Flow Control

The RTL8305S supports IEEE 802.3x full duplex flow control and half duplex back-pressure congestion control. Once the full duplex flow control ability is enabled via ENFCTRL, the Nway ability with full duplex flow control will be negotiated during the auto-negotiation process. When operating in half duplex mode, a proprietary back-pressure algorithm is enabled via the ENBKPRS pin, which can prevent traditional hub devices from partition due to excessive collisions. For MII port applications, the same functions will be applied to port4 depending on the state of P4FLCTRL# and P4DUPSTA#. If port4 is not configured to MII port application, it acts as a UTP port and behaves according to the configuration of the ENFCTRL and ENBKPRS pins.

6.2.6 Back-off Algorithm

The RTL8305S implements the truncated exponential back-off algorithm compliant to the 802.3 standard. The collision counter will be reset after 16 consecutive collisions, which leads to a smaller back-off time.

6.2.7 Inter-Frame Gap

The Inter-Frame Gap is 9.6us for 10Mbps Ethernet and 960ns for 100Mbps Fast Ethernet.

6.2.8 Illegal Frame

Illegal frames such as CRC error packets, runt packets (packet length less than 64 bytes) and oversize packets (packet length greater than 1536 bytes) will be discarded.

6.2.9 Broadcast Storm Control

The RTL8305S processes broadcast storm control via the latched value of the EnBrdCtrl pin upon reset. Once enabled, the incoming consecutive broadcast packets will be discarded after consecutive 64 broadcast packets are received during an 800ms time window. Any non-broadcast packets can reset the time window and broadcast counter such that the scheme restarts.

6.3 Physical Layer Functional Overview

6.3.1 Auto-negotiation

The RTL8305S obtains the states of duplex, speed and flow control ability through the auto-negotiation mechanism, defined in IEEE802.3u specifications, for each UTP port. During auto-negotiation, each port advertises its ability to its link partner and compares ability with those received from its link partner. By default, the RTL8305S advertises full capabilities (100Full, 100Half, 10Full, 10Half) together with flow control ability.

Asserting NWAYHALF# sets the Nway ability of the RTL8305S to half duplex only (100Half, 10Half). Deasserting ENFCTRL sets the Nway ability without the flow control function. ENBKPRS is a pin to enable the half duplex flow control scheme, which is defined in auto-negotiation. The MII port obtains its duplex, speed, flow control and link states from pins as described in section 5.5.

6.3.2 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded and driven into the network medium. The internal filter shapes the driven signals to reduce EMI emission, eliminating the need for an external filter.

6.3.3 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects that the signal level has exceeded the configured squelch level.

6.3.4 Link Monitor

The 10Base-T link pulse detection circuit always monitors the RXIP/RXIN pins for the presence of valid link pulses. Auto-polarity is implemented to correct the detected reverse polarity of RXIP/RXIN signal pairs.

6.3.5 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT3 encoding. After 4B/5B coding, the 5-bit serial data stream is scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be significantly reduced.

The scrambled seed is unique for each port, based on PHY addresses. After scrambling, the bit stream is driven into the network medium in the form of MLT-3 signaling. Multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also benefits EMI emission issues.

6.3.6 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits, to compensate for the incoming distortion of the MLT-3 signal, MLT-3 to NRZI, NRZI to NRZ converter to convert analog signaling to a digital bit-stream, and a PLL circuit to clock data bits precisely with minimum bit error rate. The de-scrambler, 5B/4B decoder and serial-to-parallel conversion circuits follow. Finally, the converted parallel data is fed into the MAC.

6.3.7 Power Saving Mode

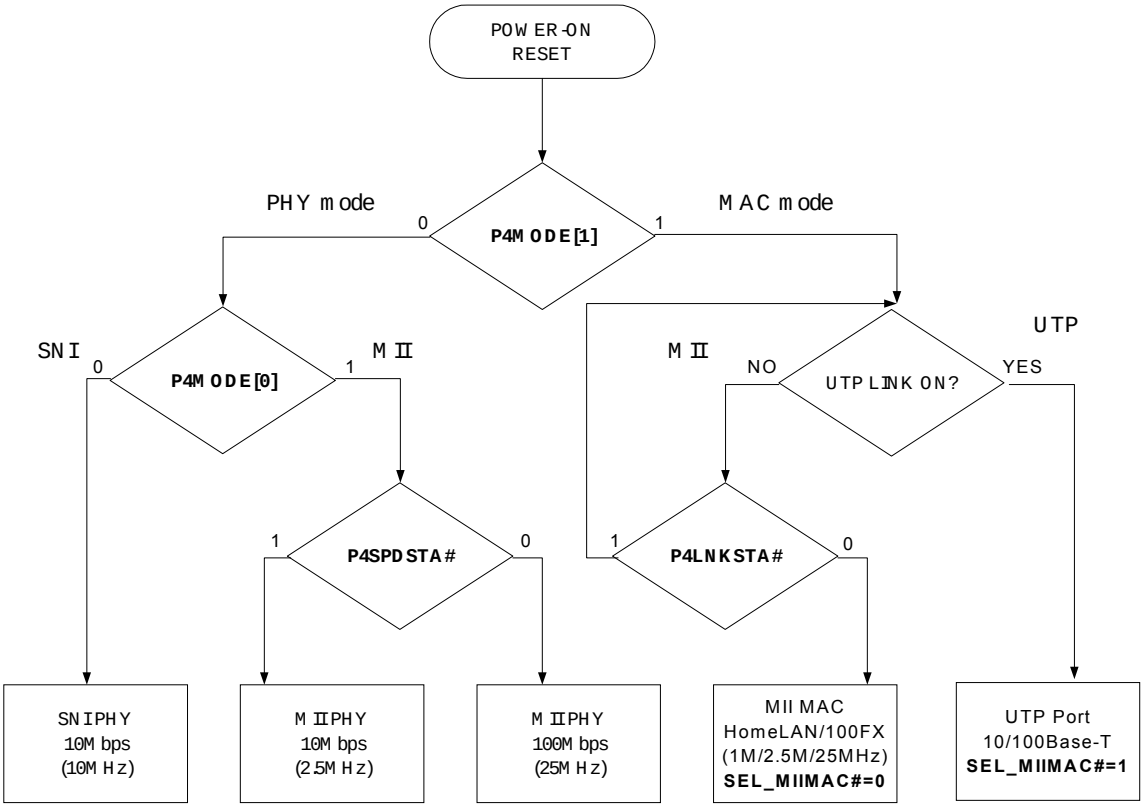
The RTL8305S implements power saving mode on per port basis. A port automatically enters power saving mode 10 seconds after the cable is disconnected from it. Once a port enters power saving mode, it transmits normal link pulses only on its TXOP/TXON pins and keeps monitoring RXIP/RXIN to try to detect any incoming signals, which might be a 100Base-TX MLT-3 idle pattern, 10Base-T link pulses or Nway's FLP (Fast Link Pulses). After it detects any incoming signals, it wakes up from the power saving mode and operates in the normal mode according to the result of the connection.

6.4 LED

The RTL8305S supports three parallel LEDs for each port. LED_ACT indicates activity and link status, LED_DPX indicates collision and duplex status, and LED_SPD indicates operating speed with state '0' equal to 100Mbps. All LED pins are active low, and blink when presenting activity and collision states. During power-on reset, the RTL8305S supports diagnostics of chip reset and LED functions by blinking all parallel LEDs once. This function can be disabled by asserting DIS_RST_BLINK# to 0. LED_BLINK_TIME determines LED blinking period for activity and collision, with 1 = 43ms and 0 = 120ms. LEDs corresponding to port 4 can be tri-stated (disable LED functions) for MII port applications by pulling ENP4LED low.

6.5 MII Port

6.5.1 General Description



The RTL8305S supports an extra MII interface for external devices. Two modes are implemented on the MII port, MII/SNI PHY mode, and MII MAC mode. In MII/SNI PHY mode, a routing engine can connect ADSL or a cable modem to a LAN through the MII port of the RTL8305S. In MII MAC mode, other types of LAN medium can be supported such as HomePNA or 100Base-FX via the underlying physical devices through the MII port of the RTL8305S. The MII signals do not include MTXER,MRXER and MCRS for RTL8305S. MDC/MDIO signals are also not supplied. Additional pins are used to complete link, speed, duplex and flow-control settings described as follows.

When port4 is configured to something other than a UTP port, i.e. MII port is activated, four input pins, P4LNKSTSA#, P4DPXSTA#, P4SPDSTA# and P4FLCTRL# are provided to determine link, duplex, and speed statuses as well as flow control ability similar to force mode. These four pins are active low.

If P4LNKSTA#=0, the RTL8305S takes the MII port as link on, and will forward/receive packets to/from the MII port.

If P4DPXSTA#=0, the RTL8305S takes the MII port as full duplex, allowing simultaneous Tx/Rx.

If P4SPDSTA#=0, the RTL8305S takes the MII port as 100Base-TX, and outputs a 25MHz clock signal from the MTXC and MRXC pins while in MII PHY mode. If P4SPDSTA#=1, it outputs a 2.5MHz clock signal instead. For SNI PHY mode (P4MODE[1]=0, P4MODE[0]=0), both MTXC and MRXC are 10MHz clock output signals and P4SPDSTA# should be floating. For MII MAC mode (P4MODE[1]=1), MTXC and MRXC are clock inputs from the underlying physical device.

It is suggested to keep P4SPDSTA# floating for SNI PHY mode and MII MAC mode for HomePNA applications, due to the dedicated speed of these two applications.

The other active-low input pin is P4FLCTRL#, which determines if flow control algorithm is enabled through the MII port. (default P4FLCTRL#=1)

If P4FLCTRL#=0 and P4DPXSTA#=0, 802.3x flow control packets will flow through the MII port.

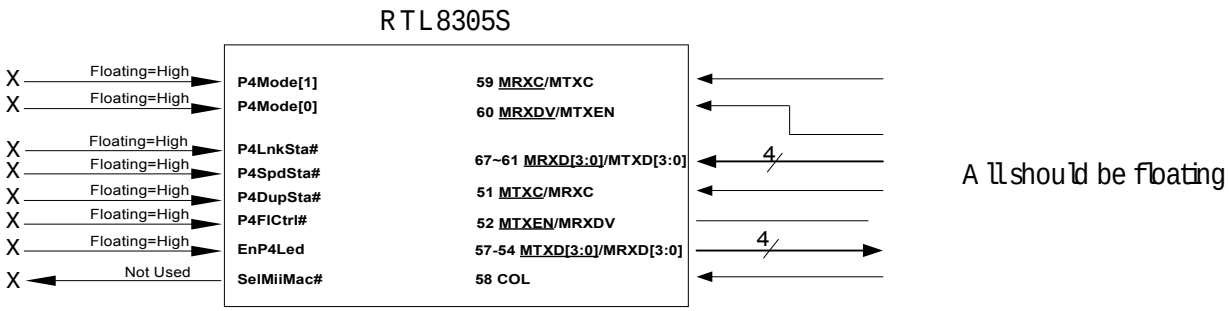
If P4FLCTRL#=0 and P4DPXSTA#=1, a back-pressure algorithm will be implemented through the MII port.

If P4FLCTRL#=1, no flow control algorithm is performed on the MII port.

All three input pins, P4DPXSTA#, P4SPDSTA#, and P4FLCTRL#, have no effect when P4LNKSTA#=1.

It is important to note that the MRXD[3:0] pins in MII/SNI PHY mode are MTXD[3:0] for MII MAC mode, and vice versa. Also the same for pin MRXDV vs. MTXEN, and pin MRXC vs. MTXC.

NOTE: There are no MRXER, MTXER, MCRS and SMI (MDC/MDIO) pins for MII signaling. Because of the absence of MCRS, system designers can wire MRXDV directly to CRS and RXDV of the opposite chip.

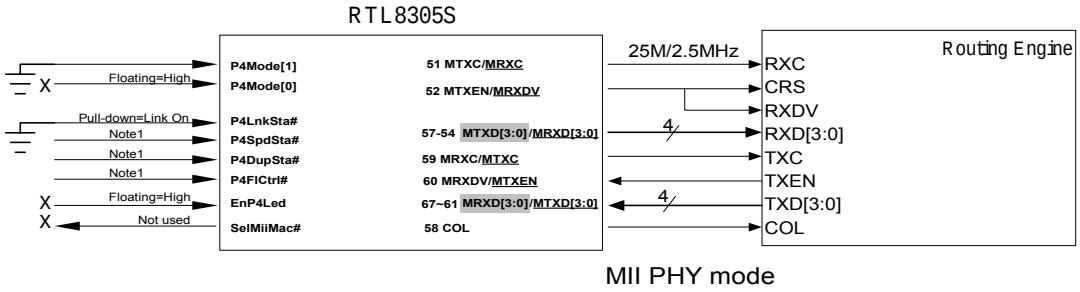


5 UTP Mode (Default five port switch application)

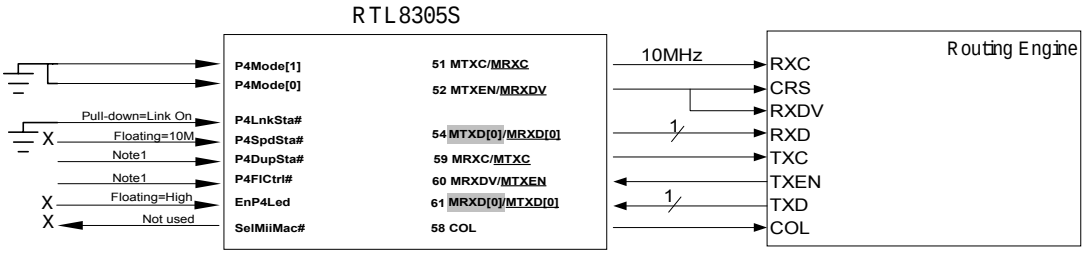
For general cases, most of the option pins should be floating (=High=Enable), except EnBrdCtrl. This means that EnBrdCtrl should be pulled down (=Low=Disable) for normal applications.

The illustrations below show a summary of MII/SNI application circuits for port4 of the RTL8305S.

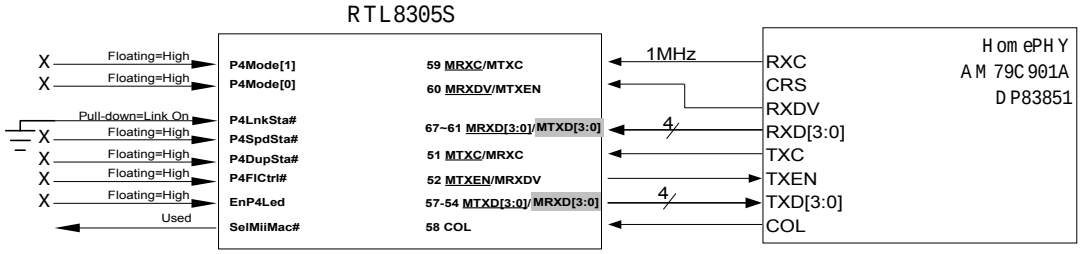
Note that, as described above, the pins MRXC, MRXDV and MRXD in MII/SNI PHY mode are pins MTXC, MTXEN and MTXD in MII MAC mode, and vice versa.



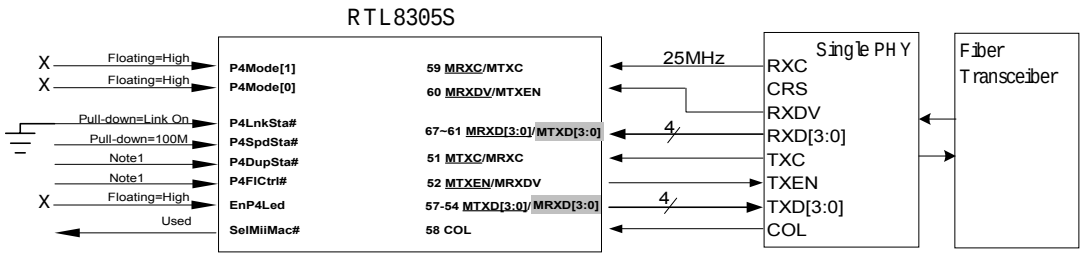
MII PHY mode



SNI PHY mode



MII MAC mode (HomePNA Application)



MII MAC mode (100Base-FX Application)

Note 1: Floating or Pull-down states depend on application.

Note 2: For general cases, most of the option pins should be floating (=High=Enable), except for EnBrdCtrl. This means that EnBrdCtrl should be pulled down (=Low=Disable) for normal applications.

6.5.2 MII/SNI PHY Mode

In routing applications, the RTL8305S cooperates with a routing engine to communicate with a WAN (Wide Area Network) through MII/SNI. In such applications, P4LNKSTA# =0 and P4MODE[1] are pulled low upon power-on reset. P4MODE[0] determines whether MII or SNI mode is selected. In MII (nibble) mode (P4MODE[0]=1), P4SPDSTA# =0 results in MII operating at 100Mbps with MTXC and MRXC running at 25MHz; however, P4SPDSTA#=1 leads to MII operating at 10Mbps with MTXC and MRXC running at 2.5MHz. In SNI (serial) mode (P4MODE[0]=0), P4SPDSTA# has no effect and must be floating. SNI mode operates at 10Mbps only, with MTXC and MRXC running at 10MHz. In SNI mode, RTL8305S does not loopback RXDV signals as a response to TXEN and does not support heart-beat functions (asserting the COL signal for each complete TXEN signal).

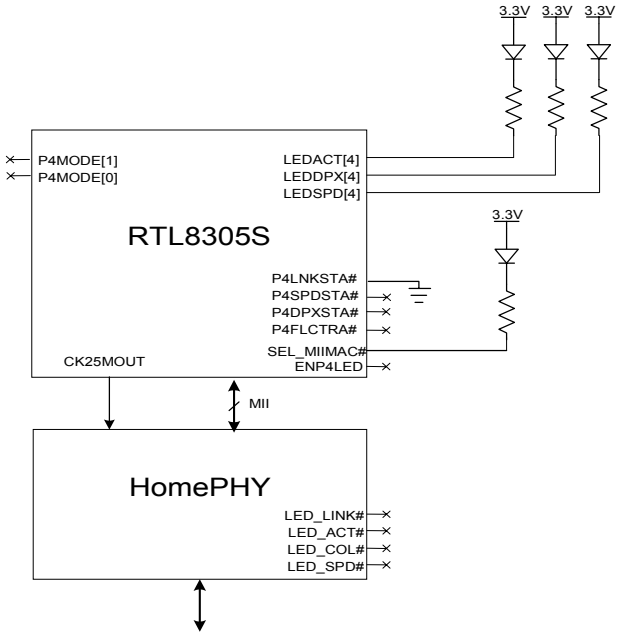
By pulling-up ENP4LED (internal default =1), the RTL8305S displays the MII/SNI status through LEDs of port 4, such as activity/link, collision/duplex, and speed.

6.5.3 MII MAC Mode

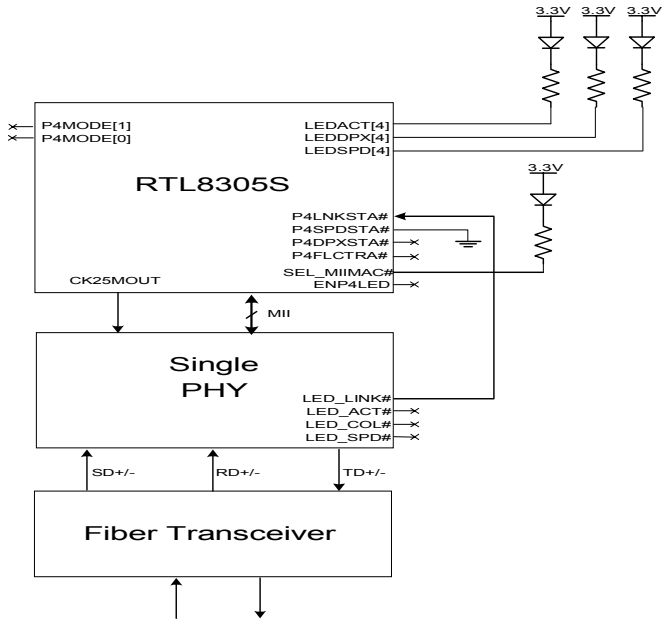
In HomePNA/100Base-FX applications, the RTL8305S provides the MII interface to the underlying HomePNA or 100Base-FX related physical devices to communicate with other types of LAN medium. In such applications, P4MODE[1] is pulled high upon power-on reset and the RTL8305S supports the UTP/MII auto-detection function. When both UTP and MII are active (link on), the UTP port has a higher priority over the MII port. In HomePNA applications, P4SPDSTA# must be floating and, since HomePNA is half-duplex only, P4DPXSTA# should be floating as well. It is recommend to pull P4LNKSTA# low instead of being wired to the LINK LED pin of the HomePHY because of the unstable link state of the HomePHY configuration, which is a characteristic based on the HomePNA 1.0 standard. For 100Base-FX applications, P4LNKSTA# =0, P4SPDSTA# =0 and P4DPXSTA# depends on the application.

By pulling-up ENP4LED (internal default =1), the RTL8305S displays the MII status through the LEDs of port 4, such as activity/link, collision/duplex, and speed. Pin SEL_MIIMAC# can be used to indicate that the MII MAC port is active by a LED for the sake of UTP/MII auto-detection. Finally, a 25MHz clock output (CK25MOUT) can be used as a clock source for the underlying HomePHY/100Base-FX physical devices.

A brief application for HomePNA and 100Base-FX is depicted below.



Common LEDs (RTL8305S driving)
MII MAC mode (UTP / HomeLAN auto-detect)



Common LEDs (RTL8305S driving)
MII MAC mode (UTP / 100Base-FX auto-detect)

As illustrated above, P4LNKSTA# needs to be pulled low to enable the MII MAC port, accompanied with P4MODE[1] pulled high. An LED connected to SEL_MIIMAC# pin can indicate whether the UTP or MII port is selected.

For 100Base-FX applications, the Link LED status pin can even be wired to P4LNKSTA# to implement the UTP/MII auto-detection feature with no need to permanently disable port4 UTP capabilities. For the RTL8305S, UTP priority takes over the MII port if both are link on.

7. Electrical Characteristics

7.1 Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified reference to GND unless otherwise specified.

Parameter	Min	Max	Units
Storage Temperature	-45	+125	°C
Vcc Supply Referenced to GND	-0.5	+4.0	V
Digital Input Voltage	-0.5	Vcc	V
DC Output Voltage	-0.5	Vcc	V

7.2 Operating Range

Parameter	Min	Max	Units
Ambient Operating Temperature(Ta)	0	+60	°C
Vcc Supply Voltage Range(Vcc)	3.15	3.45	V

7.3 DC Characteristics (0°C<Ta<60°C, 3.15V<Vcc<3.45V)

Parameter	SYM	Conditions	Min	Typical	Max	Units
Power Supply Current	Icc	10 Base-T, idle 10 Base-T, Peak continuous 100% utilization 100 Base-TX, idle 100 Base-TX, Peak continuous 100% utilization 10/100 Base-TX, low power without cable		150 610 450 500 240		mA
Power Consumption	PS	10 Base-T, idle 10 Base-T, Peak continuous 100% utilization 100 Base-TX, idle 100 Base-TX, Peak continuous 100% utilization 10/100 Base-TX, low power without cable		0.495 2.013 1.485 1.650 0.792		W
TTL Input High Voltage	V_{ih}		2.0			V
TTL Input Low Voltage	V_{il}				0.8	V
TTL Input Current	I_{in}		-50		50	µA
TTL Input Capacitance	C_{in}			5		pF
Output High Voltage	V_{oh}		Vcc-0.4			V
Output Low voltage	V_{ol}				0.4	V
LED Output Current	I_{oh}				33	mA

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Output Tristate Leakage Current	$\|I_{OZ}\|$				10	µA
Transmitter, 100Base-TX (1:1 Transformer Ratio)						
TX+/- Output Current High	I_{OH}				40	mA
TX+/- Output Current Low	I_{OL}		0			uA
Transmitter, 10Base-T (1:1 Transformer Ratio)						
TX+/- Output Current High	I_{OH}				100	mA
TX+/- Output Current Low	I_{OL}		0			µA
Transmitter, 100Base-TX (1.25:1 Transformer Ratio)						
TX+/- Output Current High	I_{OH}				32	mA
TX+/- Output Current Low	I_{OL}		0			µA
Transmitter, 10Base-T (1.25:1 Transformer Ratio)						
TX+/- Output Current High	I_{OH}				80	mA
TX+/- Output Current Low	I_{OL}		0			µA
Receiver, 100Base-TX						
RX+/- Common-mode input voltage				1.32		V
RX+/- Differential input resistance				20		KΩ
Receiver, 10BaseT						
Differential Input Resistance				20		kΩ
Input Squelch Threshold				340		mV

7.4 AC Characteristics (0°C<Ta<60°C, 3.15V<Vcc<3.45V)

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Transmitter, 100Base-TX						
Differential Output Voltage, peak-to-peak	V_{OD}	50Ω from each output to Vcc, Best-fit over 14 bit times		1.968		V
Differential Output Voltage Symmetry	V_{OS}	50Ω from each output to Vcc, |Vp+|/ |Vp-|		1		%
Differential Output Overshoot	V_{OO}	Percent of Vp+ or Vp-		3.32	5	%
Rise/Fall time	t_r,t_f	10-90% of Vp+ or Vp-	3.3	3.8	4.1	ns
Rise/Fall time imbalance	$\|t_r - t_f\|$			200	500	ps
Duty Cycle Distortion		Deviation from best-fit time-grid, 010101... Sequence		±175	±200	ps
Timing jitter		Idle pattern		0.9	1.0	ns
Transmitter, 10Base-T						
Differential Output Voltage, peak-to-peak	V_{OD}	50Ω from each output to Vcc, all pattern	4.5	5.06	5.5	V
TP_IDL Silence Duration		Period of time from start of TP_IDL to link pulses or period of time between link pulses	13.6	15.6	16	ms
TD Short Circuit Fault Tolerance		Peak output current on TD short circuit for 10 seconds		152		mA
TD Differential Output Impedance (return loss)		Return loss from 5MHz to 10MHz for reference resistance of 100 Ω	26		40	dB
TD Common-Mode Output Voltage	Ecm	Terminate each end with 50Ω resistive load		45.6	50	mV
Transmitter Output Jitter				11.5		ns
RD Differential Output Impedance (return loss)		Return loss from 5MHz to 10MHz for reference resistance of 100 Ω	35			dB
Harmonic Content		dB below fundamental, 20 cycles of all ones data	27	28		dB
Start-of-idle Pulse width		TP_IDL width	280		330	ns

7.5 Digital Timing Characteristics

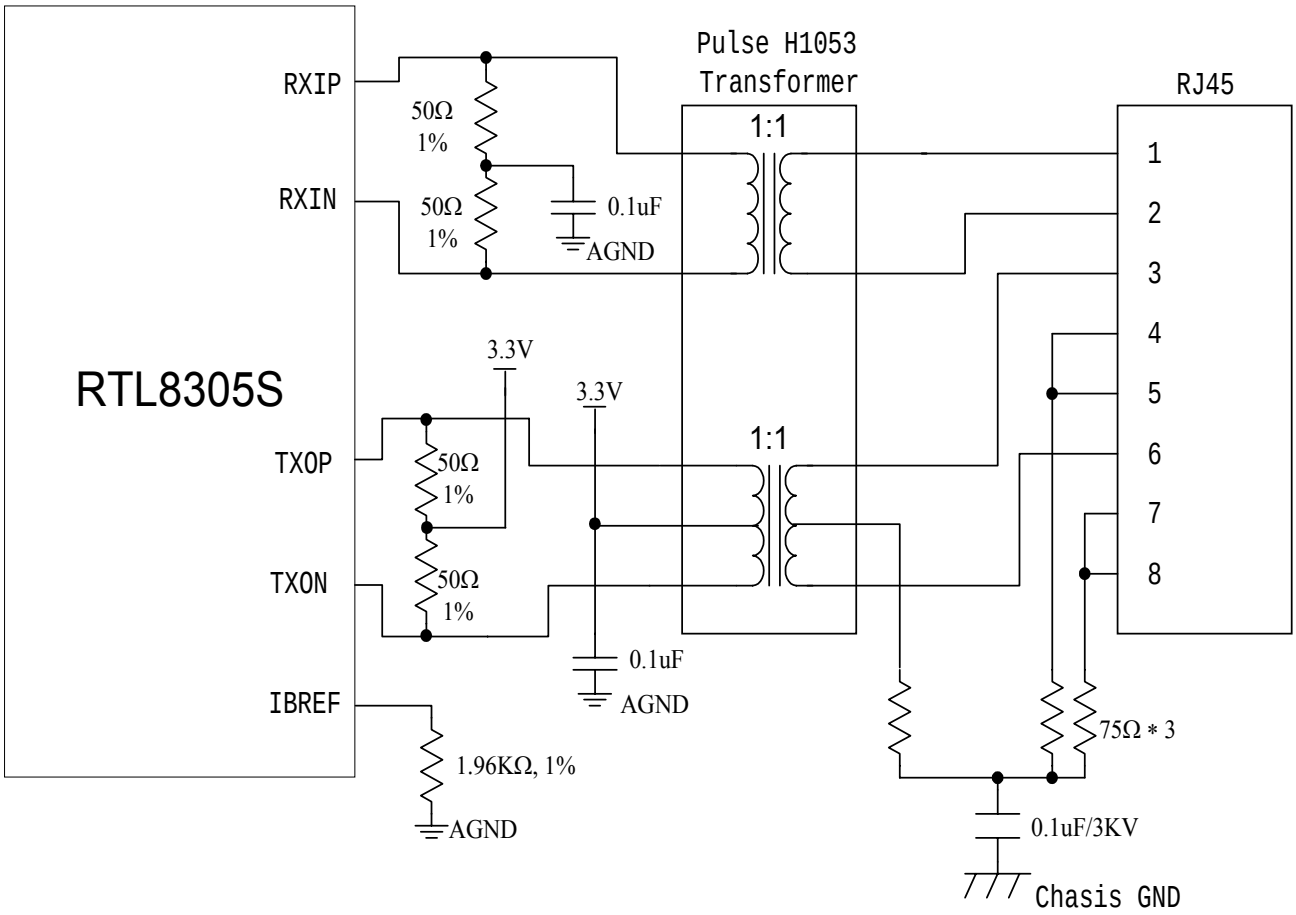
Parameter	Symbol	Conditions	Min	Typical	Max	Units
100Base-TX Transmit System Timing						
Active TX_EN Sampled to first bit of "J on MDI output						Bits
Inactive TX_EN Sampled to first bit of "T on MDI output						Bits
TX Propagation Delay	t_{TXpd}	From TXD[1:0] to TXOP/N				Bits
100Base-TX Receive System Timing						
First bit of "J on MDI input to CRS_DV assert		From RXIP/N to CRS_DV		6	8	Bits
First bit of "T on MDI input to CRS_DV de-assert		From RXIP/N to CRS_DV		16	18	Bits
RX Propagation Delay	t_{RXpd}	From RXIP/N to RXD[1:0]		15	17	Bits
10Base-T Transmit System Timing						
TX Propagation Delay	t_{TXpd}	From TXD[1:0] to TXOP/N		5	6	Bits
TXEN to MDI output		From TXEN assert to TXOP/N		5	6	Bits
10Base-T Receive System Timing						
Carrier Sense Turn-on delay	t_{CSON}	Preamble on RXIP/N to CRS_DV asserted		12		Bits
Carrier Sense Turn-off Delay	t_{CSOFF}	TP_IDL to CRS_DV de-asserted		8	9	Bits
RX Propagation Delay	t_{RXpd}	From RXIP/N to RXD[1:0]	9		12	Bits
LED Timing						
LED On Time	t_{LEDon}	While LED blinking		43		ms
LED Off Time	t_{LEDoff}	While LED blinking		43		ms
Jabber Timing (10Base-T only)						
Jabber Active		From TXEN=1 to Jabber asserted	60	70	80	ms
Jabber de-assert		From TXEN=0 to Jabber de-asserted	60		86	ms

7.6 Thermal Data

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Thermal resistance: junction to ambient, 0 ft/s airflow	θja	4 layers PCB, ambient temperature 25°C		24		°C/W
Thermal resistance: junction to case, 0 ft/s airflow	θjc	4 layers PCB, ambient temperature 25°C		3.9		°C/W

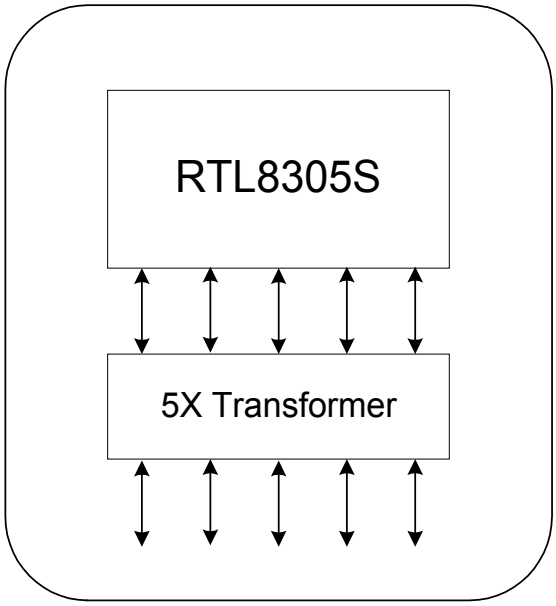
8. Application Information

UTP (10Base-T/100Base-TX) Application

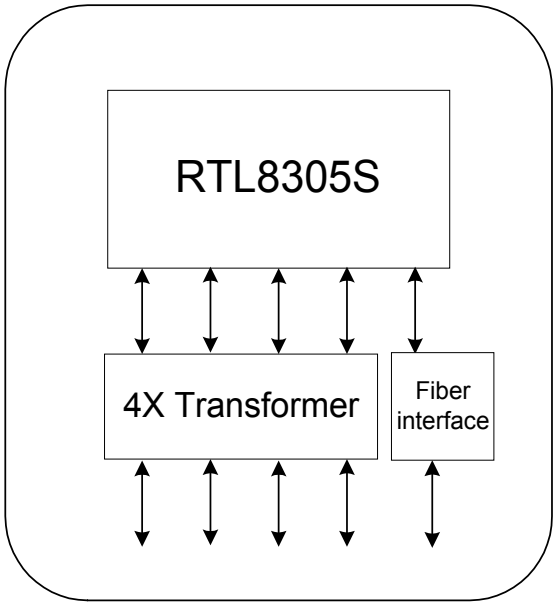


RTL8305S UTP Application

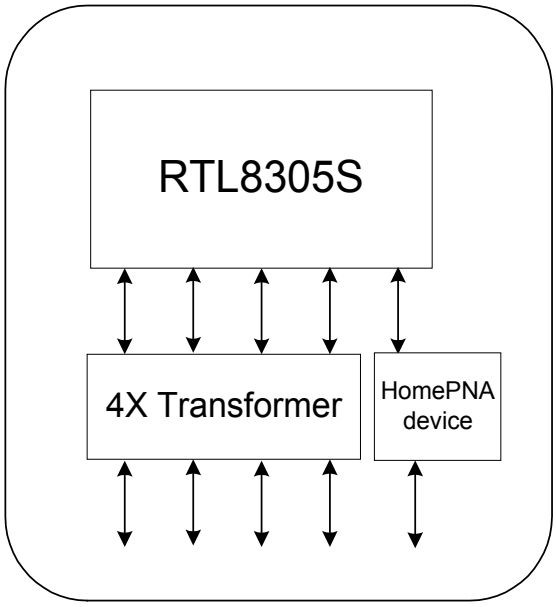
9. System Application Diagram



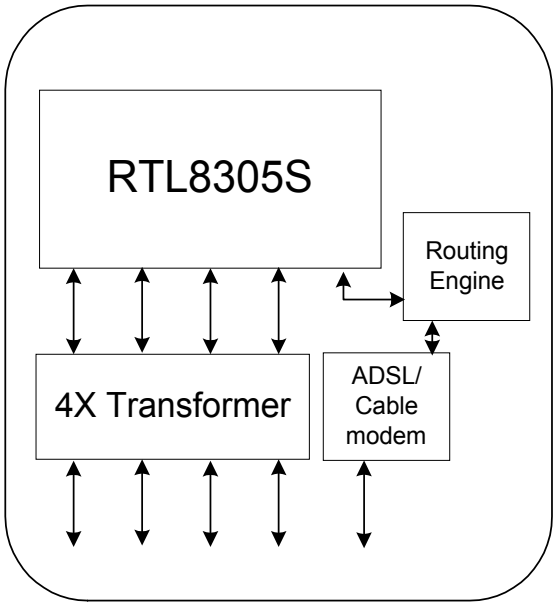
10/100Mbps x 5 UTP



10/100Mbps x 4 UTP
100Base-FX x 1

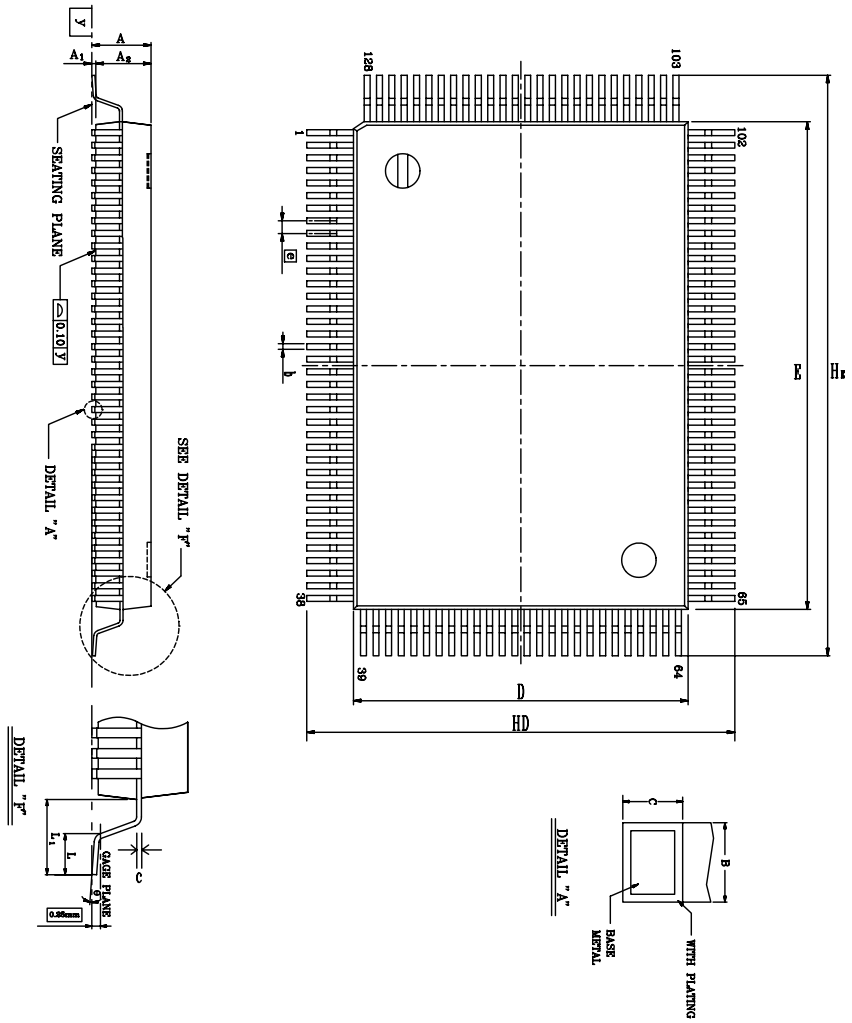


10/100Mbps x 4 UTP
HomeLAN x 1



10/100Mbps x 4 UTP
WAN x 1

10. Mechanical Dimensions



Symbol	Dimension in inch			Dimension in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.134	-	-	3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
b	0.005	0.009	0.013	0.12	**0.22**	0.32
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/ intrusion.
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.

TITLE : **128 QFP** (14x20 mm) PACKAGE OUTLINE -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL :			
APPROVE		DOC. NO.	530-ASS-P004
		VERSION	1
		PAGE	OF
CHECK		DWG NO.	Q128 - 1
		DATE	Oct. 08 1998
REALTEK SEMICONDUCTOR CO., LTD			

Document Revision Information

Revision	Date	Change
1.00	10/04/2000	Original document.
1.01	10/05/2000	Add system application diagram. P.3
1.02	10/06/2000	Add power consumption. P.20
1.03	11/15/2000	Rename TX+/- to TXOP/N and RX+/- to RXIP/N. P.5 Add pull-up 3.3V on resistors of TXOP/N. P.19
1.04	11/20/2000	Update power consumption, Power Supply Current P.20 Update AC characteristics
1.05	11/29/2000	Clarify Port4 diagram and function. P.14, P.16
1.06	12/05/2000	Clarify Pin assignment, Port4 diagram and function. P.5, P.16
1.07	12/06/2000	Update Maximum legal frame size 1728 as 1536. Update Port4 diagram and function. P.12, P.16, P.18
1.08	12/08/2000	Update Thermal Theta JA & Theta JC. P.23
1.09	12/18/2000	Add figure. Update figure note. P.15, P.16
1.10	12/22/2000	Revise 8k as 1k. P.10
1.11	01/11/2001	Revise pin name as TEST# on P.5, P.6, P.7 Revise range of Storage Temperature on P.21. Revise Ta from 70 degree C to 60 degree C on P.21 and P.22
1.12	01/19/2001	Revise aging time 300sec as Max 300 sec, Min 200 sec on P.10
1.13	01/29/2001	It is no recommended to use internal power on auto reset on P.1 P.8
1.14	02/13/2001	Clarify NwayHalf# pin description on P.7
1.15	02/16/2001	Clarify P4LNKSTA# pin description on P.7 Clarify SEL_MIIMAC# pin description on P.8
1.16	02/19/2001	Clarify Features description on P.1
1.17	05/14/2001	Clarify general description on P.1 Change Picture Item color on P.16
1.20	02/19/2002	General English adjustment.

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